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# ELECTRONIC DESIGN

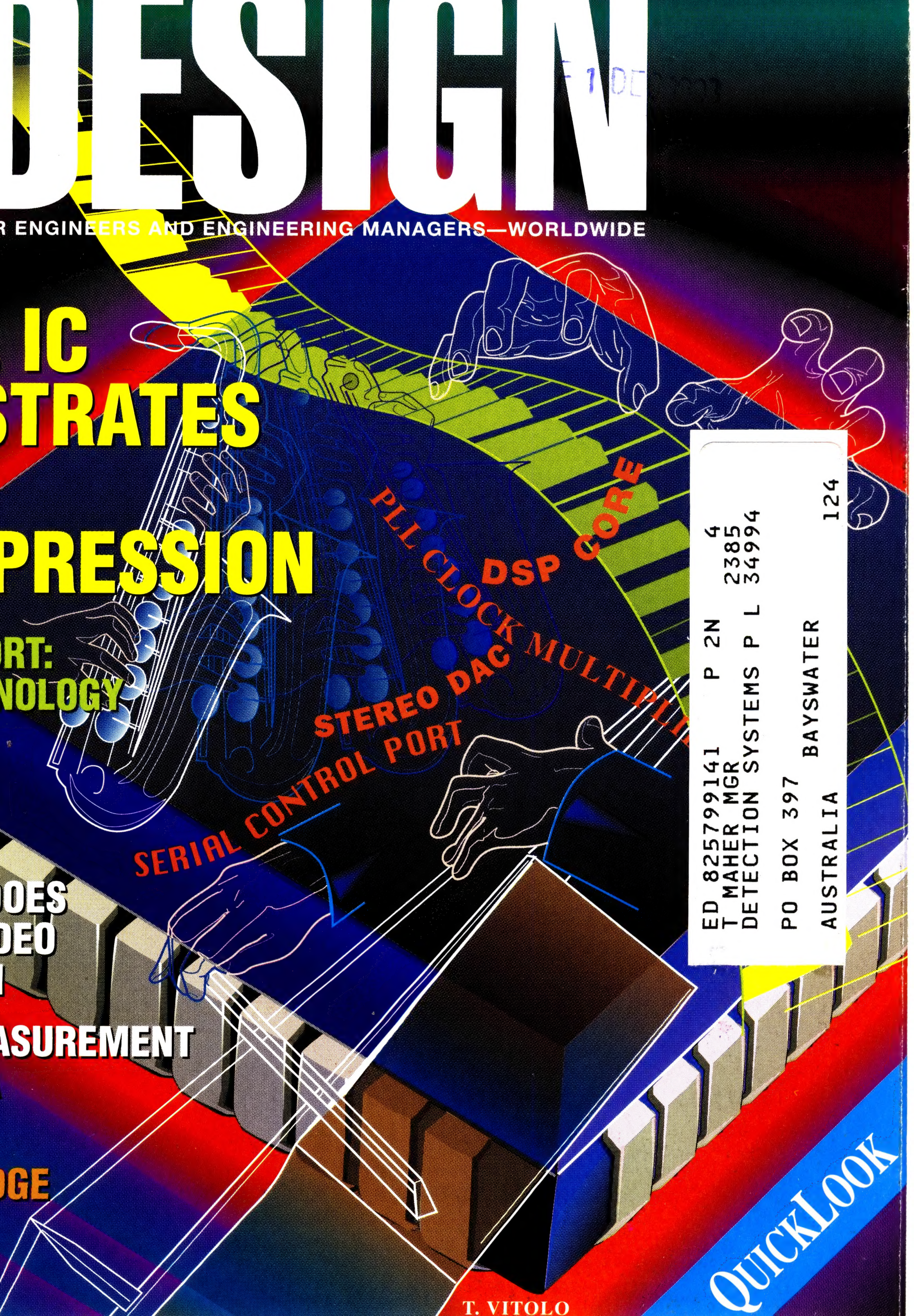
OCTOBER 1, 1993

1 DEC 1993

FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

## DIGITAL IC ORCHESTRATES AUDIO DECOMPRESSION

- SPECIAL REPORT: MODEM TECHNOLOGY
- HOW EDA SERVICES AID DESIGNERS
- SINGLE CHIP DOES REAL-TIME VIDEO COMPRESSION
- TEST AND MEASUREMENT UPDATE: DATA ACQUISITION
- PEASE PORRIDGE



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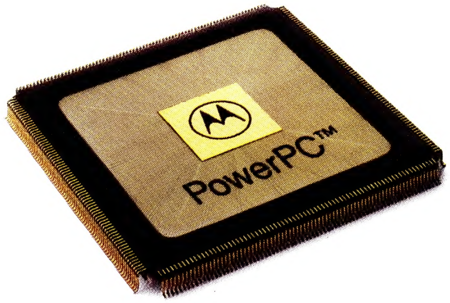

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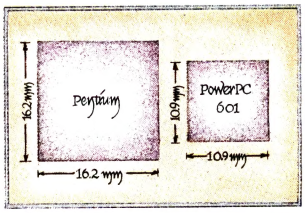

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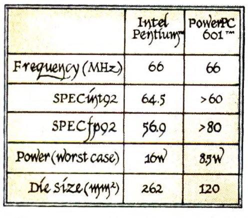

| | Intel Pentium™ | PowerPC 601™ |
|---|---|---|
| Frequency (MHz) | 66 | 66 |
| SPECint92 | 64.5 | >60 |
| SPECfp92 | 56.9 | >80 |
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formed their
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people have
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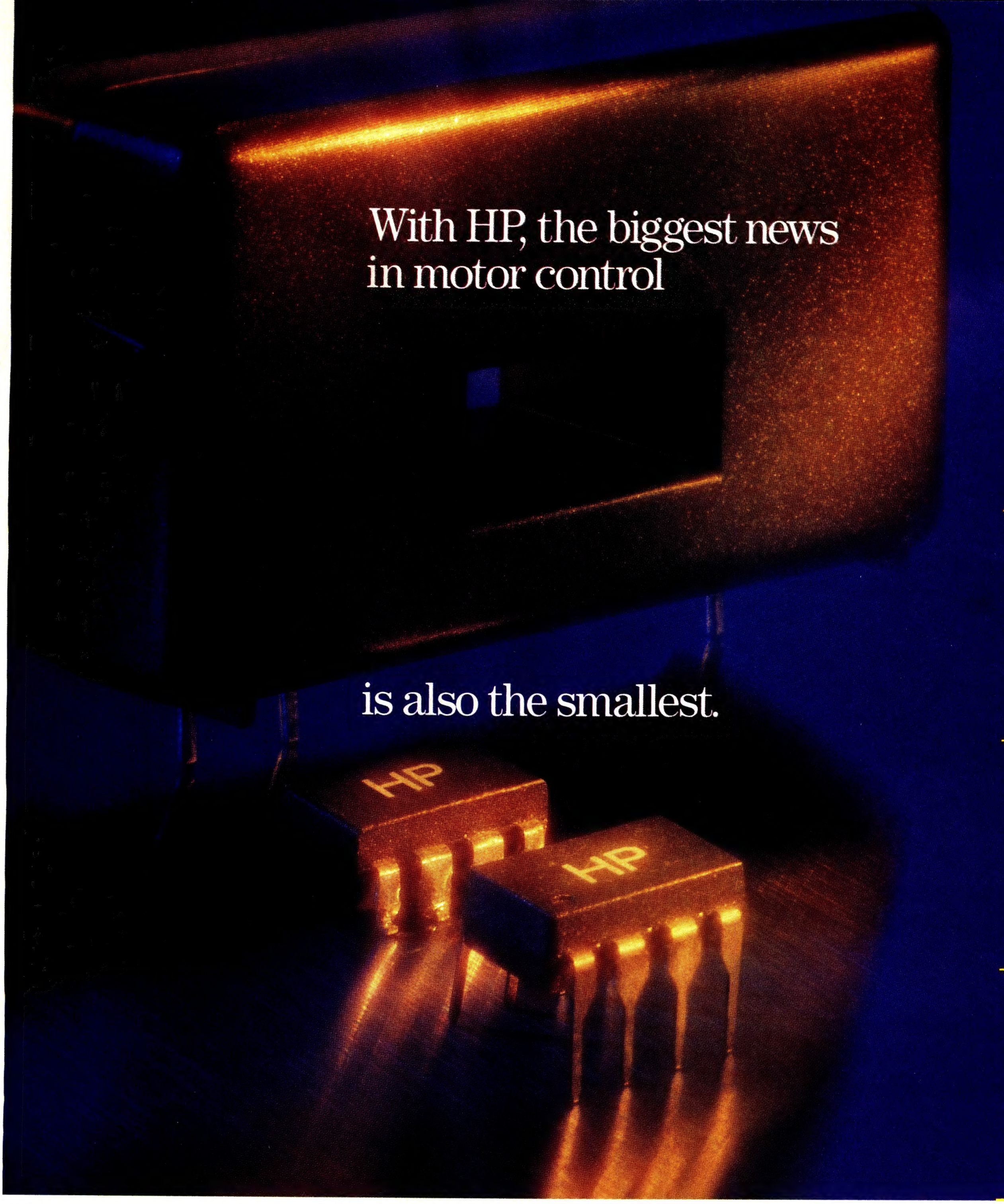
something big.



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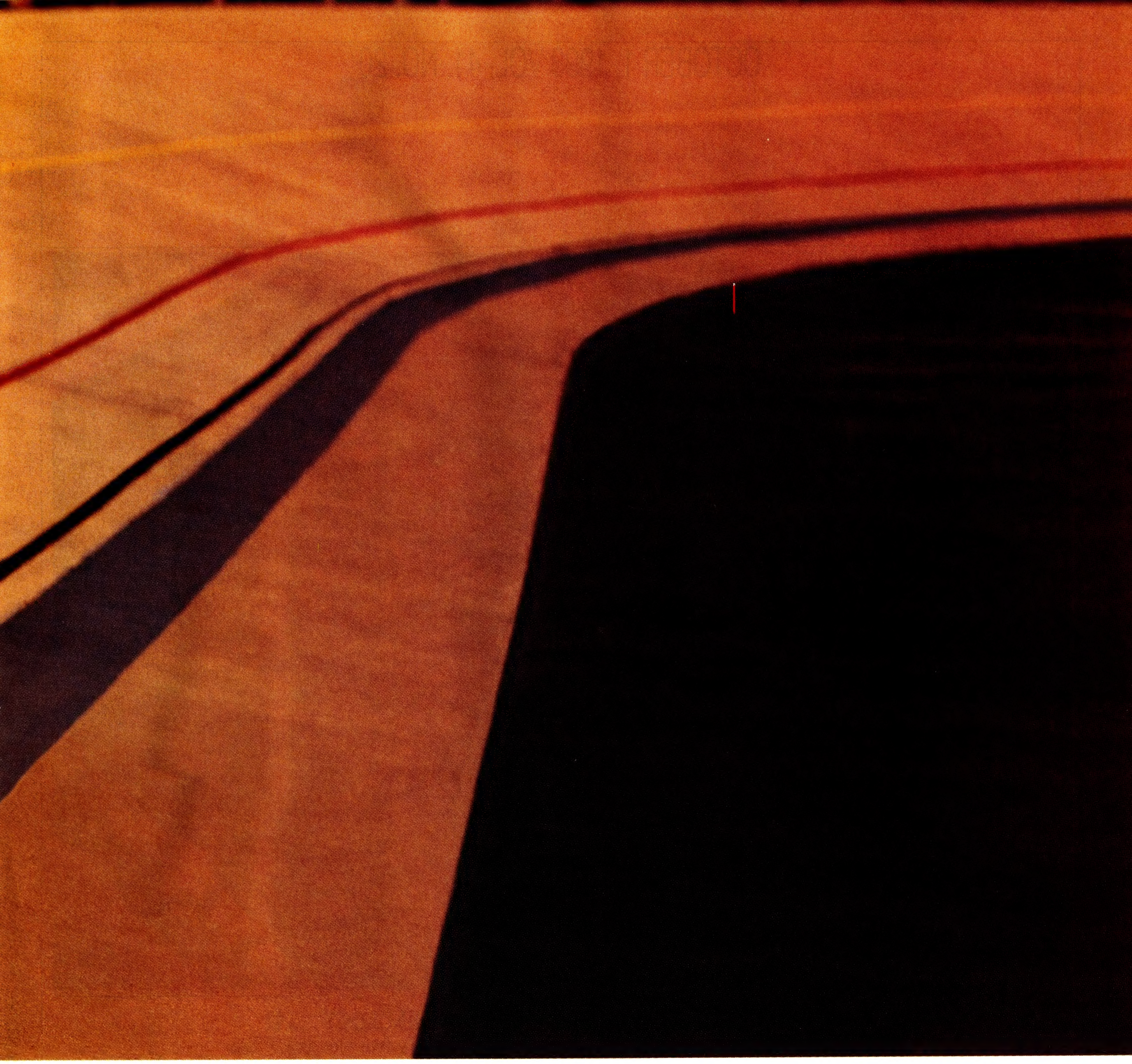

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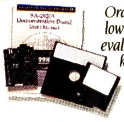

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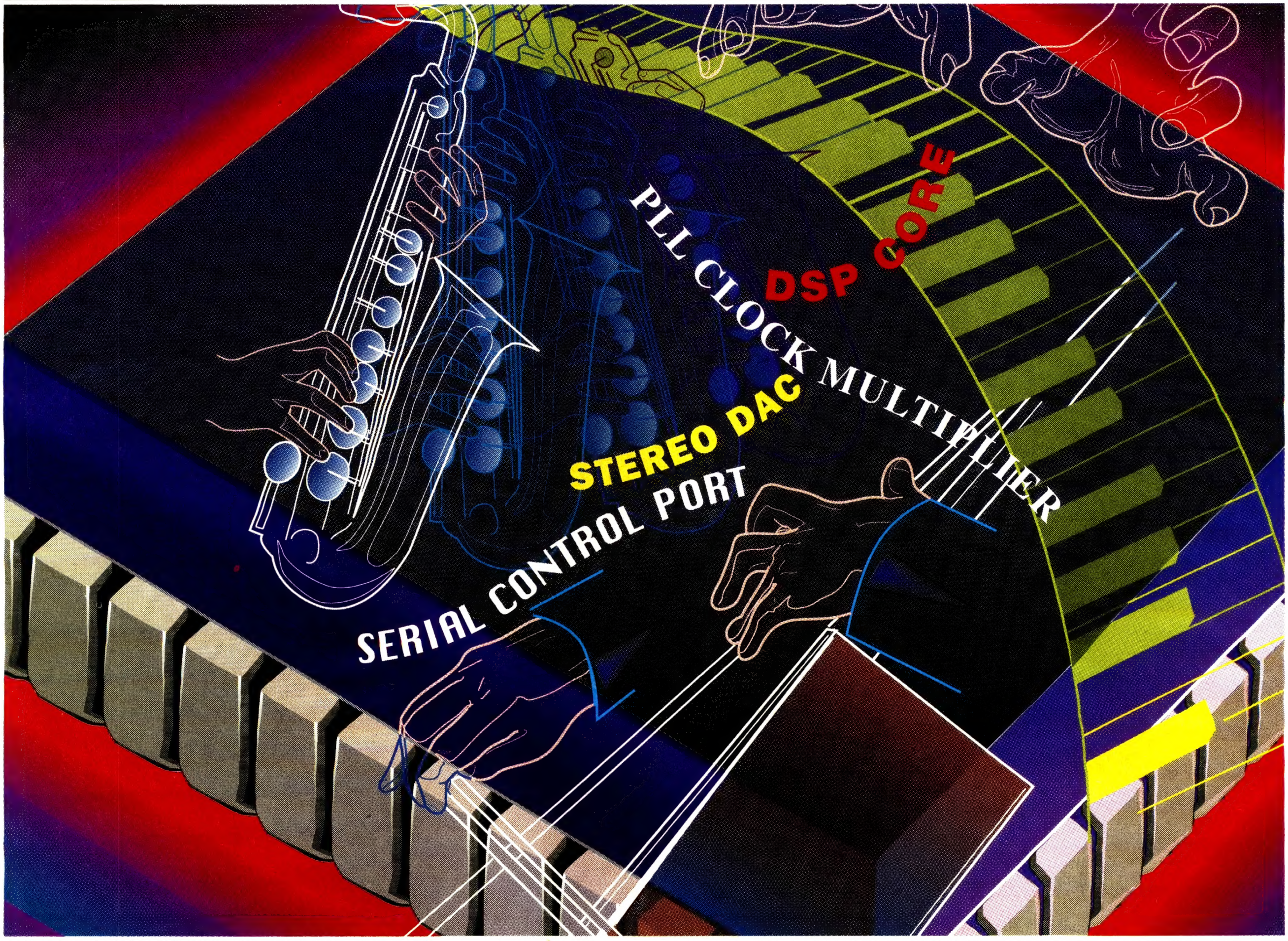

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- A new transceiver chip serves four serial interfaces
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- PLUS:

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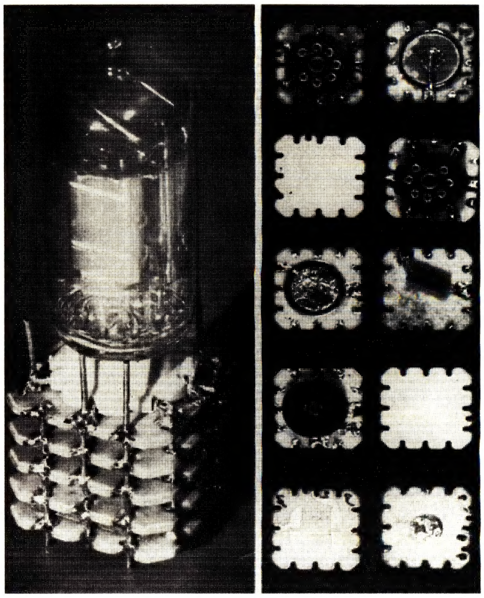
# ELECTRONIC DESIGN 40 YEARS AGO

## Project "Tinkertoy"

An automatic production line for the manufacturer of electronic equipment and a new system of electronic design which makes this possible have been developed by the National Bureau of Standards (Washington 25, D.C.) under the sponsorship of the Navy Bureau of Aeronautics. The program is known by the code name "Project Tinkertoy", and promises to have widespread application for industrial and commercial equipment as well as for military devices.

The system starts with raw or semi-processed materials, and machines automatically manufacture ceramic materials and adhesive carobe (sic—carbon?) resistors, print conducting circuits, and mount resistors, capacitors, and other miniaturized component parts on standard uniform steatite wafers. The wafers are stacked like building blocks to form a module that performs all the functions of one or more electronic stages. Automatic inspection machines check physical and electrical characteristics of the wafer units at several stages along the production line. The completed module is a standardized, interchangeable electronic subassembly that is rugged, reliable, and compact.

The design system that makes this automatic production possible is known as the MDE (Modular Design of Electronics) system. It establishes a series of mechanically standardized and uniform modules which can be produced to have a wide range of electrical characteristics. Each module usually consists of four to six thin ceramic wafers bearing various circuits associated with an electronic stage. A number of these modules are combined to form a major subassembly. The illustration shows one of the subassemblies (left), made up of ceramic wafers containing various printed and subminiature electronic components (right).



A major advantage of the "Tinkertoy" system is that it makes possible a rapid conversion from civilian to military products (and back again) on short notice. At the same time, it allows for greatly expanded production capacity. Performance of equipment made by this new system is generally equivalent to that made by conventional methods. Equipment produced on an experimental basis meets military specifications.

Several companies cooperated with the NBS in the project, including Kaiser Electronics Division of Willys Motor Co., the Doughnut Corp. of America (Ellicott City, Md.), Communication Measurements Laboratory Inc. (Plainfield, N. J.), and Sanders Associates Inc. (Nashua, N.H.). The Davis Laboratories (Riverdale, Md.) and the Navy Post Graduate School (Monterey, Calif.) also assisted in the work. *(Electronic Design, October 1953, p. 5.)*

*Project Tinkertoy was a landmark project, with its advances in component packaging density, plug-in circuit modules, and automated manufacturing. However, it had a lifetime of only a few years, primarily because it used vacuum tubes. Much smaller transistor-based modules, which in turn soon gave way to integrated circuits, rapidly made it obsolete. Side question: Does anyone have additional information on the Doughnut Corp. of America?*

*We should also mention that the October 1953 issue, in its "New Books" section, had a review of "Principles of Transistor Circuits" by Richard F. Shea (John Wiley & Sons Inc., 535 pgs., $11.00). This was the first comprehensive book on transistors and became a standard throughout the EE community.—Ed.*

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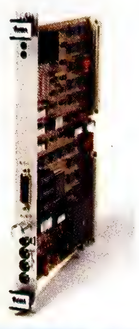

*The MMI-105 has mic and line inputs, a line output, a 56001 DSP, up to 8M bytes of RAM, and 14-bit A/D and D/A.*

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**News Editor:** Clifford Meth

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*West Coast Executive Editor:* Dave Bursky (San Jose)
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2025 Gateway Plaza, Suite 354
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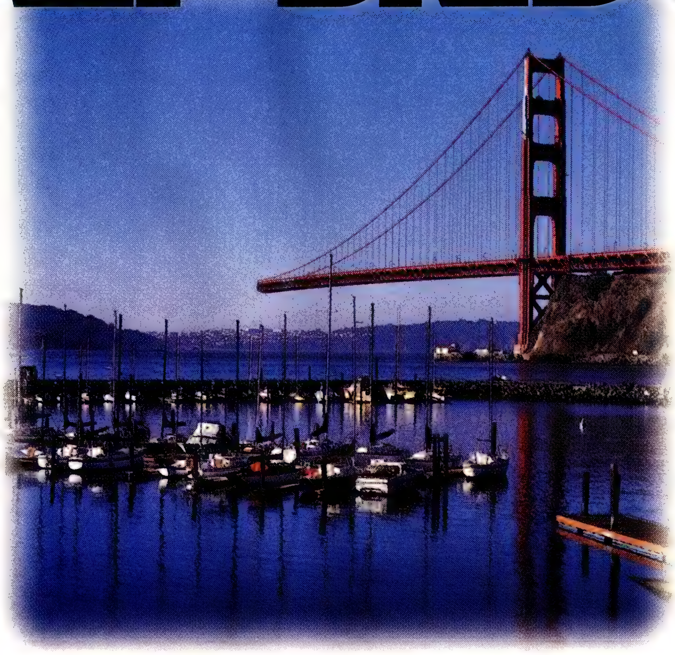

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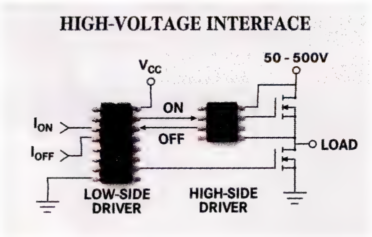

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# ELECTRONIC DESIGN

**FEBRUARY 1993**

## 165,090 Design & Development Engineers

**BASE PRICE: $100/M $145/M International**

**Design and development engineers identified by project responsibility in the OEM electronics market.**

**SOURCE:**
ELECTRONIC DESIGN magazine controlled circulation. BPA audited and updated monthly.

**JOB FUNCTION:**

| **ENGINEERING MANAGEMENT** | |
|---|---|
| Design and Development Management | 37,116 |
| Engineering Services Management | 8,653 |
| Manufacturing & Production Engineering Management | 3,176 |
| Research & Development Management | 9,108 |
| Executive Operations Management (engineering/technical) | 16,121 |
| **ENGINEERING** | |
| Design & Development | 54,855 |
| Engineering Services | 8,911 |
| Manufacturing & Production | 3,639 |
| Research & Development | 10,233 |

| **BUSINESS/INDUSTRY** | |
|---|---|
| Computers & Computer Systems | 16,836 |
| Computer Peripherals | 6,095 |
| CAE/CAD/CAM Systems | 2,011 |
| Software Manufacturer/Developer | 5,591 |
| Computer Systems Integrator | 4,484 |
| Office & Business Machines | 1,886 |
| Communications Systems & Equipment | 27,670 |
| Industrial Control Systems & Equipment | 21,787 |
| Electronic Instruments/ATE, Systems Design/Test Equipment | 12,714 |
| Medical Electronic Equipment | 7,689 |
| Avionics, Marine, Space, Military Electronics | 19,886 |
| Government & Military | 15,191 |
| Automotive, Other Ground Vehicles | 2,919 |
| Consumer Electronics, Appliances | 4,956 |
| ICs, Semiconductors | 8,189 |
| Other Components, Materials, Supplies | 3,343 |
| Electronic Sub-assemblies (boards, modules, hybrids & power supplies) | 3,843 |

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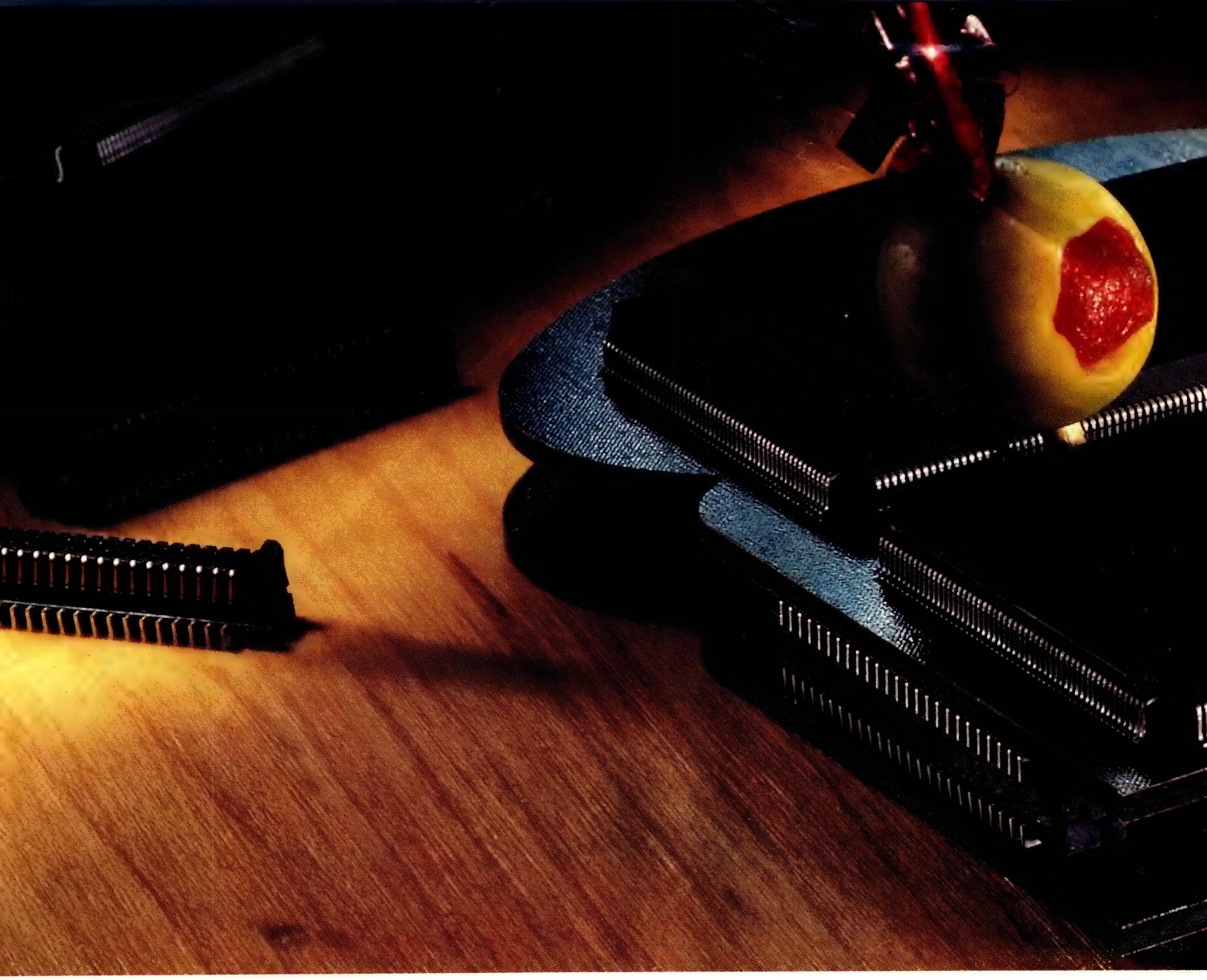
# How to sandwich more on a motherboard.

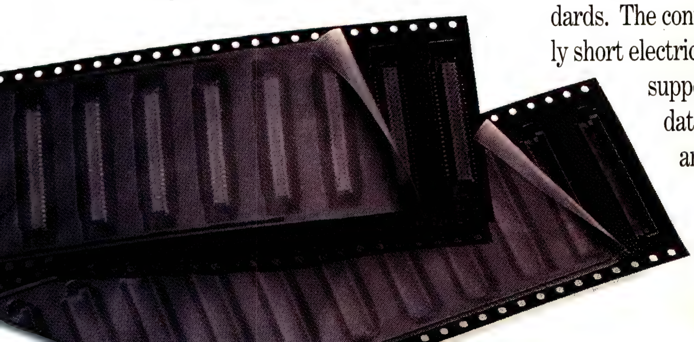


With real estate at a premium, designers are looking for new ingredients in the recipe for high-density packaging.

Enter the tasty AMPMODU Metristak interconnect family, from AMP. Designed specifically for parallel board-to-board stacking on 1.0mm centerlines, Metristak connectors offer a very high-density interface — with some very distinctive features.

A new, innovative tongue-and-groove contact design overcomes the limitations of typical pin-and-socket connectors, delivering coplanarity that exceeds industry standards. The contacts provide an exceptionally short electrical path (50 ps), capable of supporting today's demanding data rates. Simple in design and correspondingly inexpensive to produce, they're also inherently rugged: that, combined with a few special housing features, allows Metristak connectors to easily integrate with your vacuum nozzle or robotic pick-and-place machinery.

Small as they are, they're not short on user-friendliness, either. Molded-in post guides and polarizing features allow blind-mating of parallel boards — critical in tight spaces (or in the hands of non-technical end users, an increasingly important factor in today's upgradable designs).



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| 850-865 | AZ | 2,477 |
| 716-729 | AR | 254 |
| 900-961 | CA | 30,063 |
| 800-816 | CO | 2,797 |
| 060-069 | CT | 2,423 |
| 197-199 | DE | 662 |
| 200-205 | DC | 190 |
| 320-342 | FL | 4,919 |
| 300-319 | GA | 2,333 |
| 967-968 | HI | 211 |
| 832-838 | ID | 442 |
| 600-629 | IL | 5,202 |
| 460-479 | IN | 2,102 |
| 500-528 | IA | 718 |
| 660-679 | KS | 725 |
| 400-427 | KY | 437 |
| 700-714 | LA | 497 |
| 039-049 | ME | 218 |
| 206-219 | MD | 3,784 |
| 010-027 | MA | 7,019 |
| 480-499 | MI | 3,134 |
| 550-567 | MN | 2,669 |
| 386-397 | MS | 369 |
| 630-658 | MO | 1,477 |
| 590-599 | MT | 137 |
| 680-693 | NE | 389 |
| 890-898 | NV | 679 |
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| 100-149 | NY | 8,366 |
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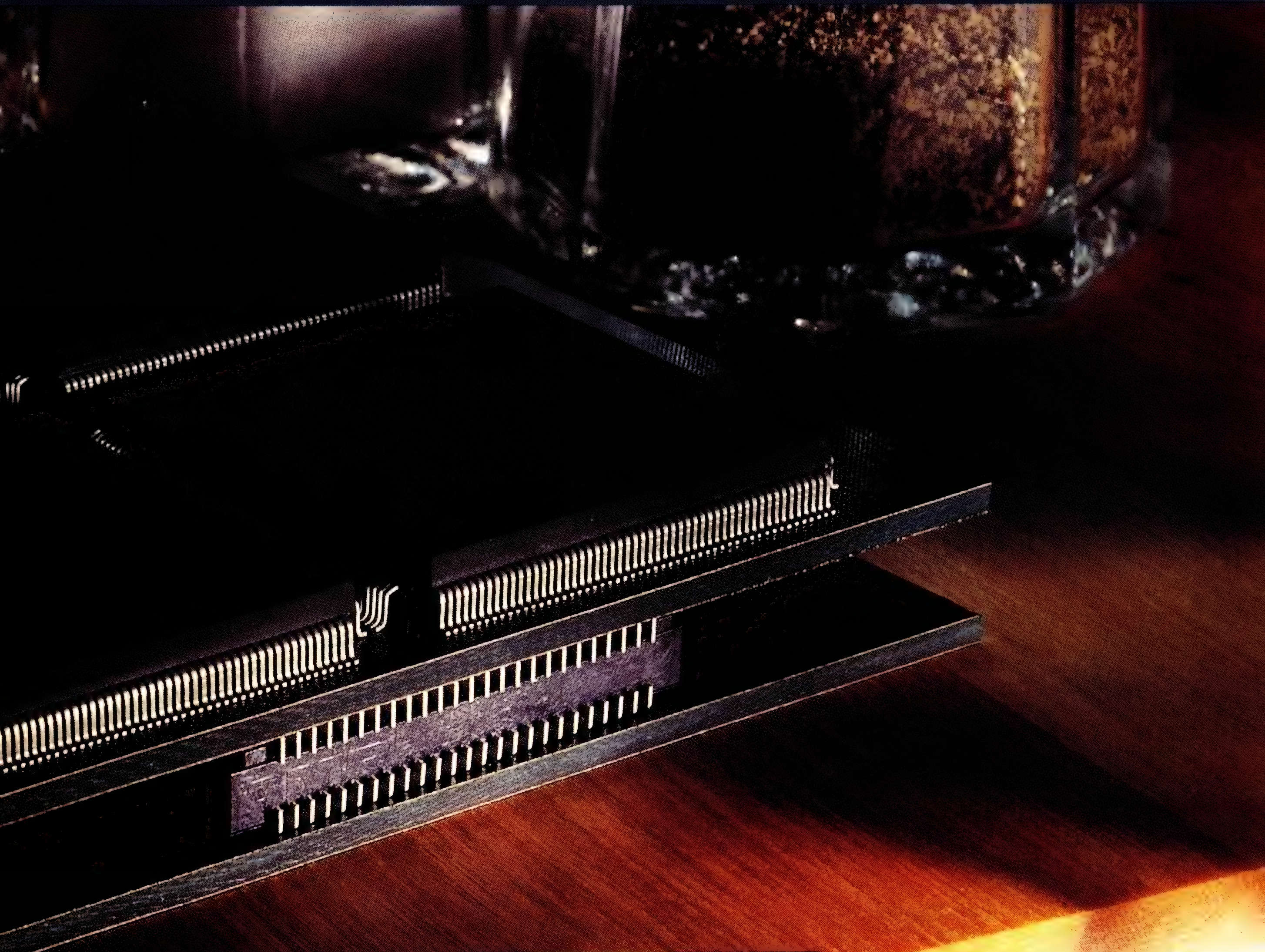
| 580-588 | ND | 89 |
| 430-458 | OH | 4,064 |
| 730-749 | OK | 826 |
| 970-979 | OR | 1,736 |
| 150-196 | PA | 4,820 |
| 028-029 | RI | 521 |
| 290-299 | SC | 658 |
| 570-577 | SD | 139 |
| 370-385 | TN | 1,039 |
| 750-799 | TX | 8,014 |
| 840-847 | UT | 1,055 |
| 050-059 | VT | 277 |
| 220-246 | VA | 3,343 |
| 980-994 | WA | 2,823 |
| 247-268 | WV | 160 |
| 530-549 | WI | 2,021 |
| 820-831 | WY | 68 |

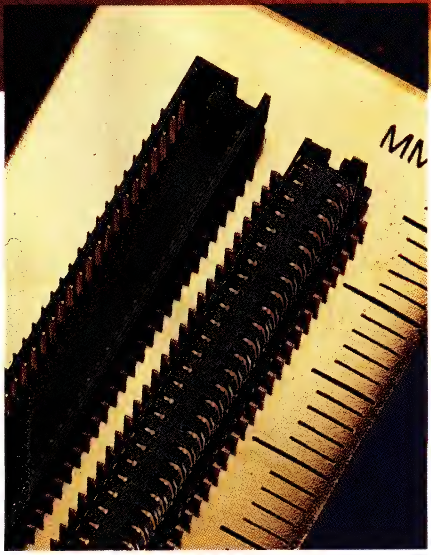
| | |
|---|---|
| **United States** | **126,962** |
| U.S. Territories | 112 |
| Canada | 2,631 |
| Central America | 75 |
| South America | 545 |
| Oceanic | 1,633 |
| Asia | 7,626 |
| Europe | 25,182 |
| Middle East | 266 |
| **FOREIGN TOTALS** | **35,385** |
| **TOTALS** | **165,090** |

Purchasing Influence by Product

| | |
|---|---|
| **Digital ICs** | |
| Microprocessor chips & support/ICs | 103,248 |
| ASCs/semicustom/custom ICs | 64,612 |
| Logic ICs | 97,837 |
| Memories | 95,278 |
| **Analog Circuits** | |
| Converter ICs & modules | 75,464 |
| Linear ICs & modules | 96,851 |
| ASCs/semicustom/custom ICs | 44,528 |
| **Components** | |
| Capacitors, resistors, potentionometers | 106,117 |
| Display devices | 92,258 |
| Relays, switches, keyboards | 94,351 |
| Motors & fans | 69,397 |
| Sensors & transducers | 78,308 |
| Microwave components & hardware | 46,542 |
| **Interconnections & Packaging** | |
| Connectors & sockets | 105,440 |
| Wire & cable | 96,140 |
| Fiber-optic cable | 51,833 |
| Enclosures | 73,638 |
| Materials | 59,449 |
| Printed circuits | 79,058 |
| **Power** | |
| Power supplies | 98,974 |
| Power semiconductor devices | 70,446 |
| Batteries | 69,920 |
| **Test & Measurement** | |
| Logic analyzers | 75,168 |
| Development systems | 66,070 |
| Oscilloscopes | 96,103 |
| Other test instruments | 78,079 |
| ATE/ASIC verifiers | 26,721 |
| Field test service equipment | 40,292 |
| **Computers & Workstations** | |
| Minicomputers | 49,981 |
| Workstations | 70,677 |
| Personal computers | 112,567 |
| **Computer Boards** | |
| CPU boards | 68,589 |
| Analog I/O boards | 60,114 |
| Other special purpose boards | 54,404 |
| **Communications** | |
| Modems | 73,474 |
| LAN hardware & software | 54,834 |
| ISDN hardware | 24,678 |
| **CAE/CAD Software** | |
| Digital/analog simulators | 52,538 |
| PC board/IC layout software | 57,159 |
| Other CAE software | 40,611 |
| **Software** | |
| Software tools, development systems & high level languages | 85,792 |
| Software packages & services | 78,115 |
| **Computer Peripherals** | |
| Disk/tape drives | 76,606 |
| Computer terminals | 67,671 |
| Graphics terminals/monitors | 68,484 |
| Printers/plotters | 84,975 |
| I/O devices | 70,468 |

Since any one subscriber may specify more than one product, the totals may exceed the total circulation. Call for merged counts.





Metristak connectors come on standard EIA481 carrier tape, ready for uncomplicated manufacturing. We'll help there, too, with all the technical support you need.

And if you need help in more basic ways, we can shorten *your* design cycle and cut your time to market with services that range from design verification to routing, board layout/fabrication to complete system architecture — taking full advantage of design breakthroughs like the Metristak interconnect family.

**For more information, call the AMP Information Center near you.**

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# THE QUALITY MESSAGE IS RECEIVED

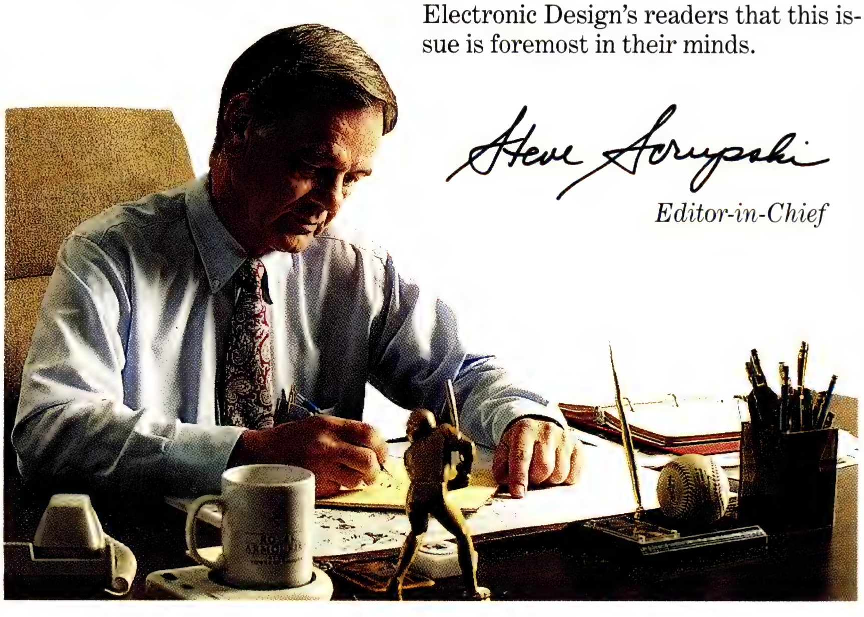
Whenever we talk to vendors these days, one subject always seems to come up: time to market. Now, we believe that time to market is key in assuring whether a product will succeed in today's fast-paced business. Needless to say, much of the material appearing in Electronic Design is aimed at helping designers meet time-to-market goals. However, we should not lose sight of a more important element of success: quality. The readers of Electronic Design, in fact, rate quality as the most important issue facing them in current design projects, even more important than time to market and design for manufacturability.

Our recent survey of Electronic Design's readers underscores this point. The survey was devised to gather various facts about our readers—age, salary, purchasing authority, etc.—as well as their opinions on various issues important in today's industry (we'll report fully on the results in a future issue). In one section of the survey, we asked readers to rate the importance of eight current industry issues on a scale of 1 to 5, with 5 being the most important. The results show that 58.8% of respondents rated designing higher quality products a 5, and 35.5% rated it a 4. Thus, 94.3% of the readers felt that quality is most important or at least very important; only 5.7% rated it a 3 (moderately important) or less. Falling in second and third behind quality were design for manufacturability (76.7% of readers rated it a 5 or 4) and time to market (70.3%).

These three issues are closely interrelated—time to market and design for manufacturability have an obvious relationship, while quality is the overriding factor in all facets of the design and manufacturing process. In some ways, you could define quality as a strategic objective and time to market and design for manufacturability as tactical goals that contribute to higher quality.

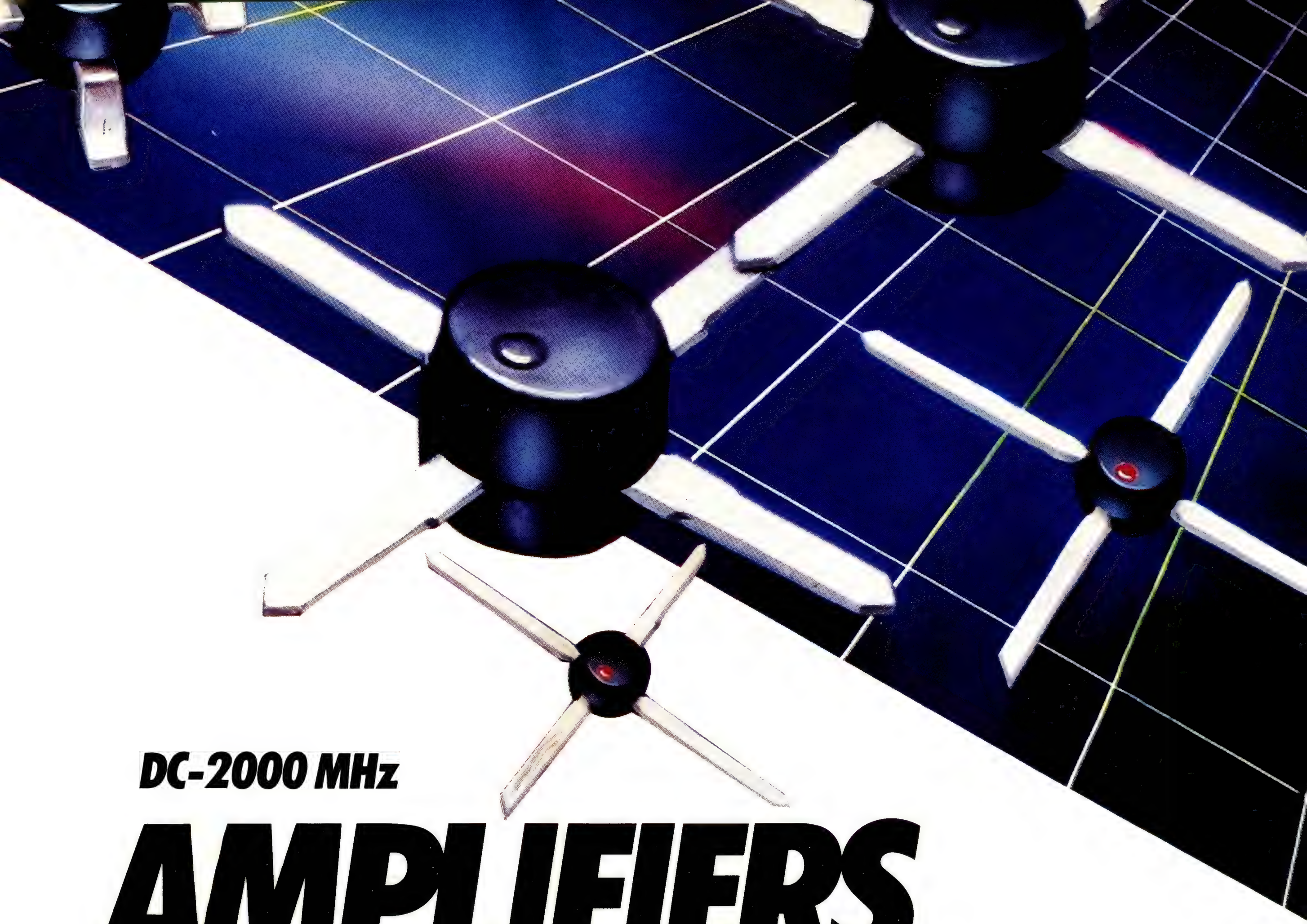
What does all this mean? Simply judging from the survey's results, it means that the quality message has been received clearly at the design level. A few years ago, when the Malcolm W. Baldrige awards were established, everyone seemed to be jumping on the quality bandwagon, touting their quality programs and lacing their speech with Baldrige-isms. Now that the initial flurry of excitement and ballyhoo about the Baldrige award has quieted, so has the bombastic talk about quality. But less talk may mean that more action is taking place. Only those who are really intent on improving quality are talking seriously about it and their TQM and 6-sigma programs.

Sure, it's easy to be in favor of quality, but it's another matter to undertake the discipline required to make a quality program work. It speaks well of Electronic Design's readers that this issue is foremost in their minds.



Steve Scrupski

*Editor-in-Chief*



## DC-2000 MHz

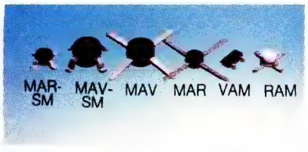
# AMPLIFIERS

**In plastic and ceramic packages,** for low-cost solutions to dozens of application requirements, select Mini-Circuits' flatpack or surface-mount wideband monolithic amplifiers. For example, cascade three MAR-2 monolithic amplifiers and end up with a 25dB gain, 0.3 to 2000MHz amplifier for less than $4.50. Design values and circuit board layout available on request.

It's just as easy to create an amplifier that meets other specific needs, whether it be low noise, high gain, or medium power. Select from Mini-Circuits' wide assortment of models (see Chart), sketch a simple interconnect layout, and the design is done. Each model is characterized with S parameter data included in our 740-page RF/IF Designers' Handbook.

All Mini-Circuits' amplifiers feature tight unit-to-unit repeatability, high reliability, a one-year guarantee, tape and reel packaging, off-the-shelf availability, with prices starting at 99 cents.

Mini-Circuits' monolithic amplifiers...for innovative do-it-yourself problem solvers.



Models above shown actual size

from **99¢** Unit price $ (25 qty)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| PLASTIC SURFACE-MOUNT | | | ++VAM-3<br>1.45 | | +VAM-6<br>1.29 | ++VAM-7<br>1.75 | | |
| add suffix SM to model no. (ex. MAR-ISM) | MAR-1<br>1.04 | MAR-2<br>1.40 | MAR-3<br>1.50 | MAR-4<br>1.60 | MAR-6<br>1.34 | MAR-7<br>1.80 | MAR-8<br>1.75 | |
| | MAV-1<br>1.15 | +MAV-2<br>1.45 | +MAV-3<br>1.55 | MAV-4<br>1.65 | | | | MAV-11<br>2.15 |
| CERAMIC SURFACE-MOUNT | RAM-1<br>4.95 | RAM-2<br>4.95 | RAM-3<br>4.95 | RAM-4<br>4.95 | RAM-6<br>4.95 | RAM-7<br>4.95 | RAM-8<br>4.95 | |
| PLASTIC FLAT-PACK | MAV-1<br>1.10 | +MAV-2<br>1.40 | +MAV-3<br>1.50 | +MAV-4<br>1.60 | | | | MAV-11<br>2.10 |
| | MAR-1<br>0.99 | MAR-2<br>1.35 | MAR-3<br>1.45 | MAR-4<br>1.55 | MAR-6<br>1.29 | MAR-7<br>1.75 | MAR-8<br>1.70 | |
| Freq.MHz,DC to | 1000 | 2000 | 2000 | 1000 | 2000 | 2000 | 1000 | 1000 |
| Gain, dB at 100MHz | 18.5 | 12.5 | 12.5 | 8.3 | 20 | 13.5 | 32.5 | 12.7 |
| Output Pwr. +dBm | 1.5 | 4.5 | 10.0 | 12.5 | 2.0 | 5.5 | 12.5 | 17.5 |
| NF, dB | 5.5 | 6.5 | 6.0 | 6.5 | 3.0 | 5.0 | 3.3 | 3.6 |

Notes: + Frequency range DC-1500MHz ++ Gain 1/2 dB less than shown

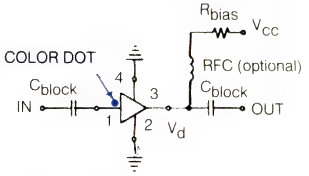
designer's amplifier kits
***DAK-2:*** 5 of each MAR-model (35 pcs), only $59.95
***DAK-2SM:*** 5 of each MAR-SM model (35 pcs) only $61.95
***DAK-3:*** 3 of each MAR, MAR-SM, MAV-11, MAV-11SM (48 pcs) $74.95

designer's chip capacitor kit
***KCAP-1:*** 50 of 17 values, 10pf to 0.1µf (850 pc), $99.95

chip coupling capacitors at .12¢ each (50 min.)

| Size (mils) | Value |
|---|---|
| 80 x 50 | 10, 22, 47, 68, 100, 220, 470, 680 pf |
| 80 x 50 | 1000, 2200, 4700, 6800, 10,000 pf |
| 120 x 60 | .022, .047, .068, .1µf |

Typical Circuit Arrangement



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F154 REV. A

# WHO

*Who made the great monoliths on Easter Island?*

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And the first company worldwide to equal the top BiCMOS speed standard. Which gives you, for the first time, an alternate source for 1-meg SRAMs at a blazing 10ns.

As a reliable, high-volume supplier, we're going to do a lot for your ability to design new products.

We'll follow the 10ns part with an even greater accomplishment — the world's first 1-meg at 8ns.

At Samsung, we're proud to be part of these advancements. And proud to extend the leadership we earned with the world's first 16-meg DRAM.

What we've done in SRAMs has been widely noticed, and we've become a supplier of choice to many of the major systems companies. Now, you can choose Samsung as your partner.

**FAST SRAM FAMILY**

| Density | Part Name | Org. | Access Time (ns) | Package | Availability | Remarks |
|---|---|---|---|---|---|---|
| 4M | KM644002 | 1M ×4 | 15/20/25 | SOJ(R) | '93,2Q | |
| | KM684002 | 512K×8 | 15/20/25 | SOJ(R) | '93,2Q | |
| | KM6164002 | 256K×16 | 20/25 | SOJ(R) | '93,3Q | |
| | KM64V4002 | 1M ×4 | 20/25 | SOJ(R) | '93,2Q | 3.3V |
| | KM68V4002 | 512K×8 | 20/25 | SOJ(R) | '93,2Q | 3.3V |
| | KM616V4002 | 256K×16 | 25 | SOJ(R) | '93,3Q | 3.3V |
| 1M | KM64B1003 | 256K×4 | 10/12 | SOJ(R) | NOW | BiCMOS |
| | KM68B1002 | 128K×8 | 10/12 | SOJ(R) | NOW | BiCMOS |
| | KM641003 | 256K×4 | 15 | SOJ(R) | NOW | |
| | KM681002 | 128K×8 | 15 | SOJ(R) | NOW | |
| | KM6161002 | 64K×16 | 15 | SOJ(R) | NOW | |
| | KM64V1003 | 256K×4 | 15 | SOJ(R) | '93,3Q | 3.3V |
| | KM68V1002 | 128K×8 | 15 | SOJ(R) | '93,3Q | 3.3V |
| | KM616V1002 | 64K×16 | 15 | SOJ(R) | '93,3Q | 3.3V |
| | KM741006 | 256K×4 | 10/12.5 | SOJ(R) | NOW | Syn. |

(R): Revolutionary Pin Configuration

**Low Power SRAM FAMILY**

| Density | Part Name | Org. | Access Time (ns) | Package | Availability | Remarks |
|---|---|---|---|---|---|---|
| 4M | KM684000 | 512K×8 | 55/70/85/100 | DIP/SOP/ TSOP | NOW | |
| | KM684000-V | 512K×8 | 75/85/100 | DIP/SOP/ TSOP | NOW | 3.3V |
| | KM658512 | 512K×8 | 80/100 | SOP/TSOP | NOW | Pseudo |
| 1M | KM681000 | 128K×8 | 70/85/100 | DIP/SOP/ TSOP | NOW | |
| | KM658128 | 128K×8 | 80/100 | DIP/SOP | NOW | Pseudo |

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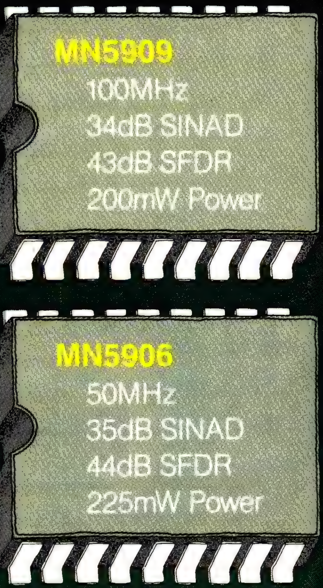

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# HIGHLY INTEGRATED CPUS SET NEW FIRSTS

Hot on the heels of new CPU announcements by Cyrix and IBM (ELECTRONIC DESIGN, *Sept. 2, p. 28*) came a second burst last month: Digital Equipment Corp. and the team of Intel Corp. and VLSI Technology Inc. each came up with CPU chips that raise the levels of system integration. The flurry of CPU releases, along with others coming this month, is being driven by three continuing trends in systems ever-higher throughput, continual cost reduction, and shrinking board space.

Trying to satisfy these requirements, DEC unveiled two highly integrated 64-bit Alpha CPU chips—the first CPUs to directly include the peripheral-component-interconnect (PCI) bus on the same chip as the processor. And, addressing the reduced-chip-count and low-power needs, the Intel-VLSI team introduced an application-tuned 386-based chip set called Polar. Compaq Computer Corp. plans to use the set in a family of "mobile companions" scheduled for 1994.

The new Alpha chips, the 21066 and 21068, employ the same core CPU as the original Alpha processor, but also include the PCI bus interface, a phase-locked-loop frequency multiplier to simplify system clocking, DRAM and cache control logic, and a graphics accelerator that provides a high-bandwidth data path to VRAM-based video memory. The 21066, which targets desktop systems, runs at 166 MHz. It delivers about 70 integer SPECmarks and about 105 floating-point SPECmarks.

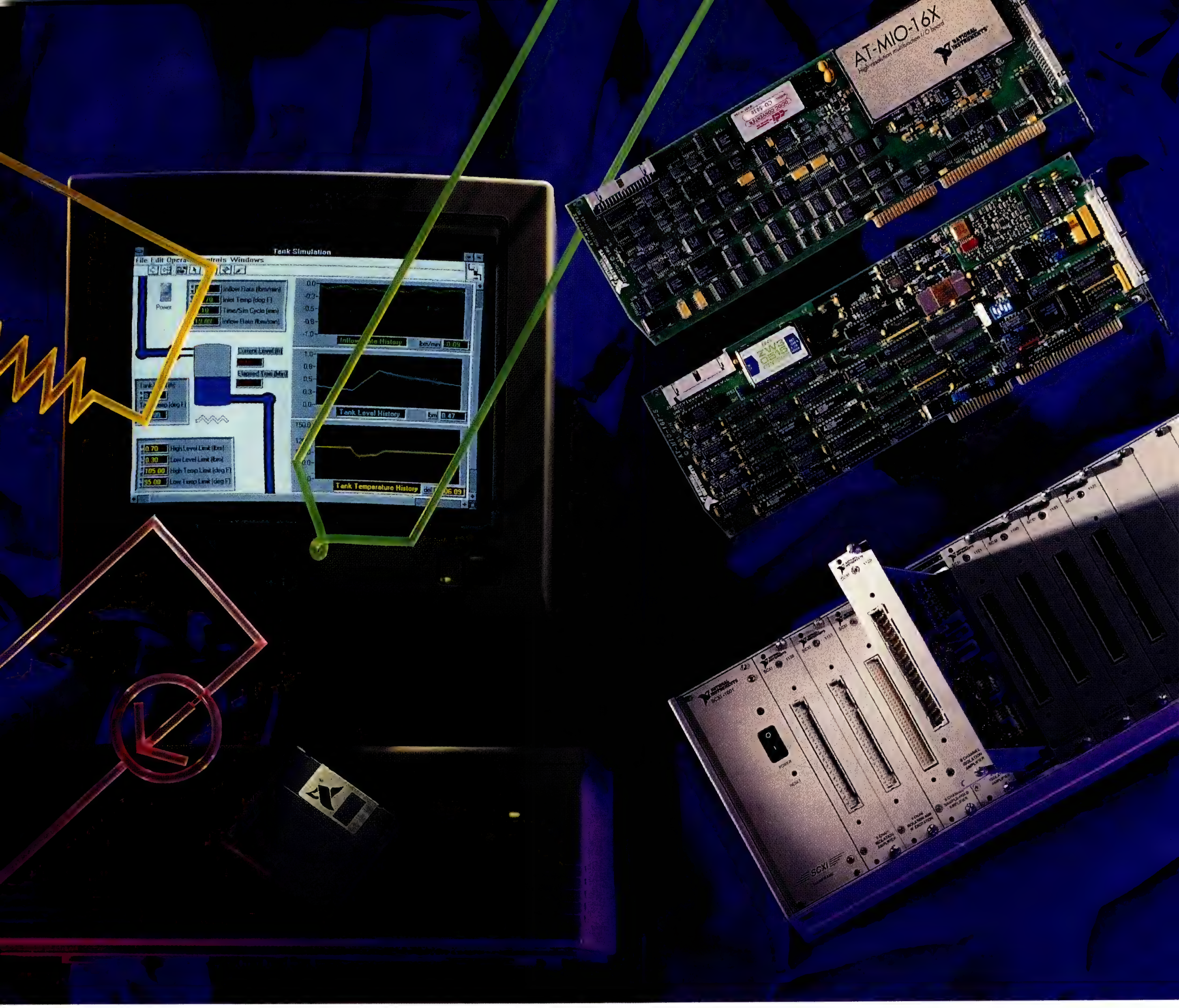
The 21068 is basically the same chip, but clocked at a reduced rate—just 66 MHz. That trims the CPU's active power from about 20 W to 8 W, making the chip more attractive for embedded-control applications. The slower clock, however, reduces the 21068's performance to 30 integer and 50 floating-point SPECmarks, still respectable numbers and better than most other high-end controllers.

DAVE BURSKY
SEMICONDUCTORS

Integration levels are also catching up with the 80386, thanks to the joint efforts of Intel and VLSI Technology. The Polar two-chip set merges the processor with all required control and support logic for a handheld system. The operating system for the Polar chips will be developed jointly by Microsoft, Compaq, Intel, and VLSI. The first chip (the VL86C300) starts with the static 80386SL CPU as the core and surrounds it with 2 kbytes of write-through cache, a two-word-deep posted-write buffer, and DRAM control circuits. Other resources include a non-multiplexed data- and address-bus interface for non-volatile memories and SRAMs, a 16-bit multiplexed local-bus (ML-bus) interface for I/O functions like PCMCIA controllers, and a 640-by-480-pixel, 16-gray-scale LCD interface with a graphics accelerator and separate ink plane.

The companion chip (the VL86C100) contains a keyboard port, a pair of interrupt controllers, two serial ports (one is compatible with Hewlett-Packard's infrared serial link scheme, which VLSI licensed from HP), and a real-time clock. Additional features include a pen-input digitizer with a 32-bit input FIFO, a three-channel 8-bit analog-to-digital converter (ADC) and a 10-bit successive-approximation ADC. The digital-to-analog converter used in the ADC also provides an audio output. To reduce parts count, the main system memory doubles as a dumb, linear frame buffer, eliminating the video memory.

Though the activity involving high-integration processors has been intense, it marks just the beginning of an approaching landslide of these devices. Later this month, for example, the joint efforts of Integrated Device Technology Inc. and Toshiba America Electronic Components Inc. will result in a highly integrated 64-bit RISC processor. Advanced Micro Devices Inc. will unveil a highly integrated 386-based chip aimed at PDAs, and Advanced RISC Machines will introduce its ARM7 enhanced processor. Many of these processors will be detailed at the upcoming 1993 Microprocessor Forum, Oct. 18-20 in Burlingame, Calif. (for conference details, call MicroDesign Resources, 707-824-4004.



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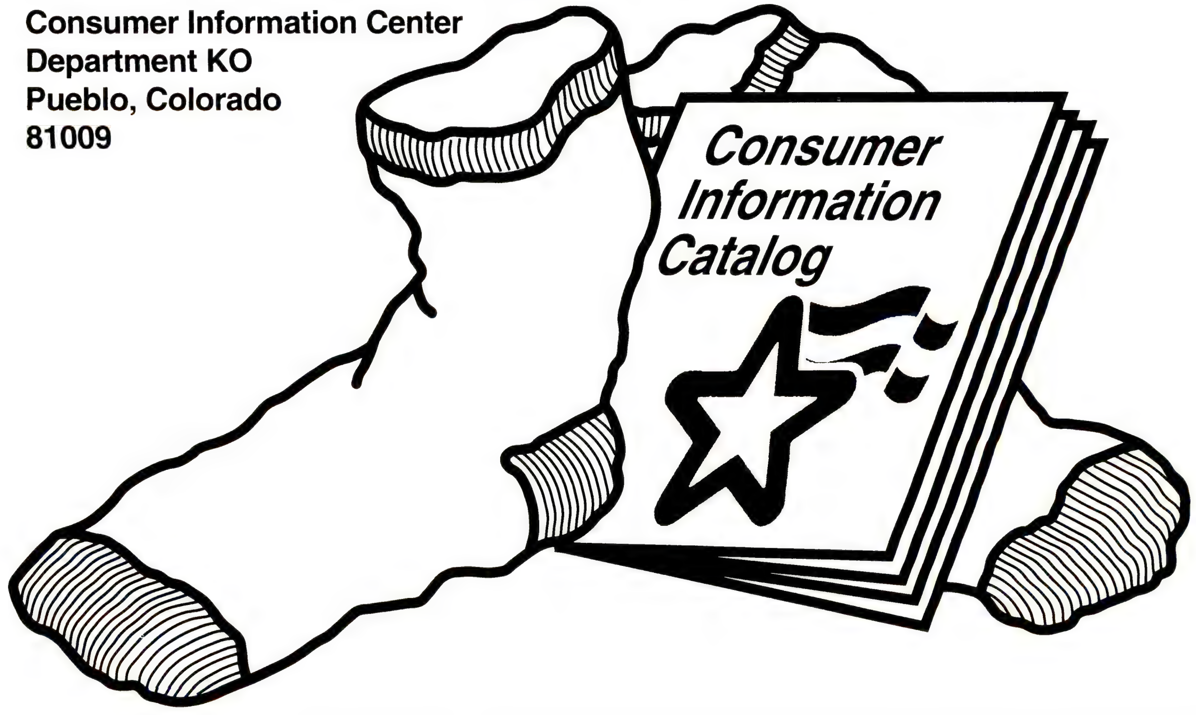

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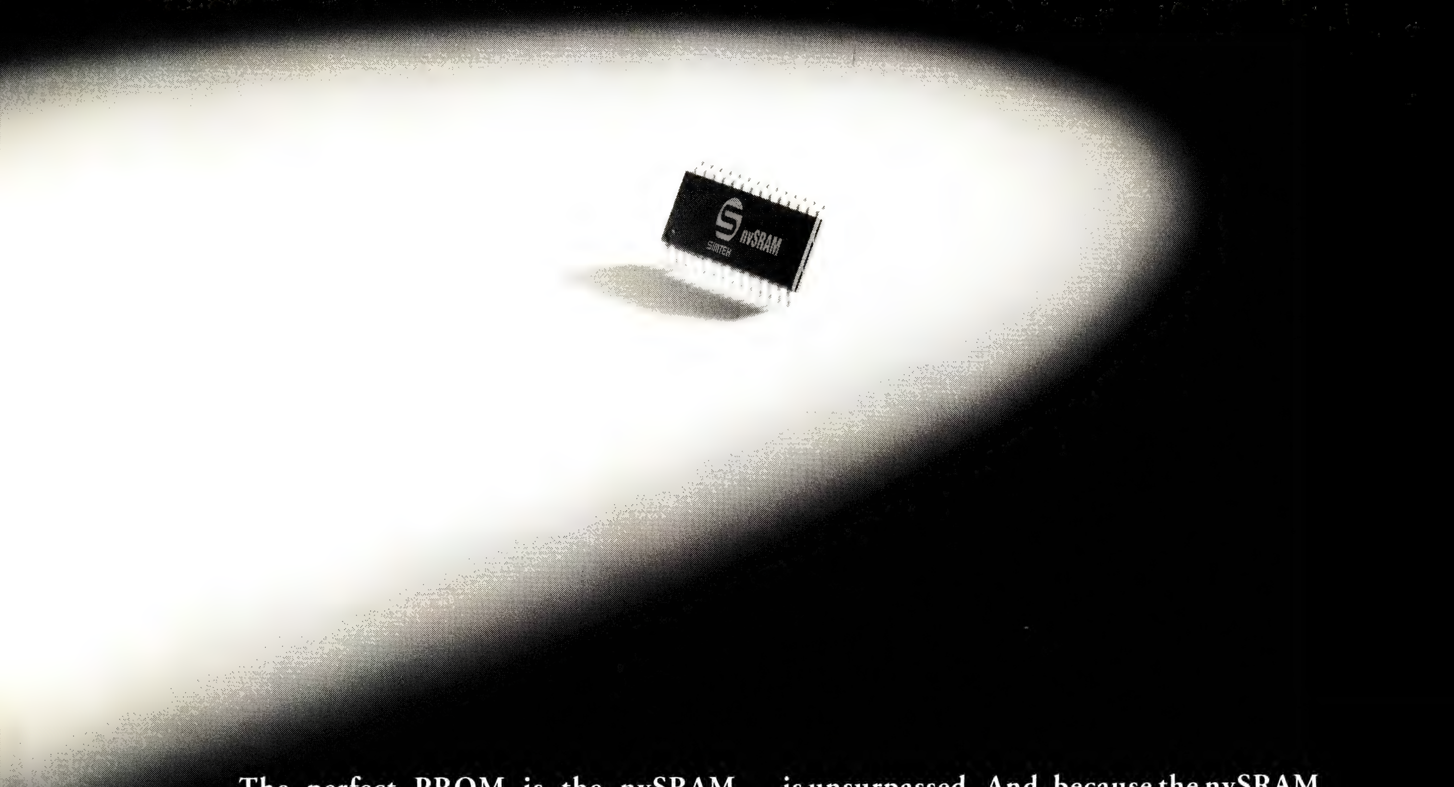

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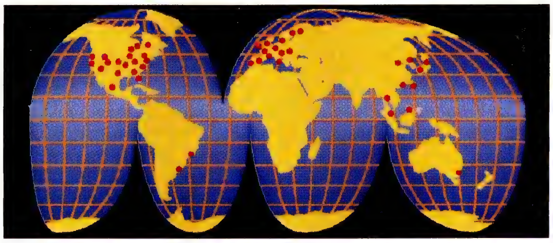

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# TECHNOLOGY NEWSLETTER

## PARALLEL PROCESSING POWERS EM SIMULATION

Boosting the power of electromagnetic (EM) simulation with parallel processing can expand its applications. For example, aircraft may be sensitive to EM influences, such as high-intensity radiated fields (HIRFs) or lightning. Traditionally, only extensive testing on the finished aircraft could detect problems. But EM simulation software that runs on a massively parallel computer can detect potential hazards while still in the design stage. Such capability is available from a package assembled by Electro Magnetic Applications Inc., Lakewood, Colo.; Finite Element Graphics Systems Inc., Duluth, Ga.; and Parsytec Inc., West Chicago, Ill. The package consists of three-dimensional EM simulation software and a field-analysis modeler that's used for preprocessing, automatic mesh generation, post processing, and data visualization. A Transputer-based parallel-processing computer developed by Parsytec runs the software. Users can model EM effects on an aircraft to significantly high frequencies, enabling the simulation of both lightning and HIRF. For instance, the system can model EM interaction (exterior and interior simultaneously) of an entire Boeing 737 aircraft up to about 1 GHz with geometry features as small as 2 in. The package can be used in many other applications that include EM effects, such as EM compatibility and antenna analysis. For more information, call Parsytec's Reinhard Rinn at (708) 293-9500. *LM*

## CONSORTIUM TO DEVELOP STANDARD ANALOG HDL

The U.S. Air Force's Rome Laboratory has awarded a development contract for an analog hardware-description language (AHDL) to a consortium led by MTL Systems Inc., Dayton, Ohio. The proposed AHDL will describe the physical design, electrical behavior, logical structure, and system-annotation information for analog circuits. Plans are to coordinate the standardization of this language with the IEEE. In fact, an important goal of the effort is to ensure compatibility with the IEEE VHDL digital standard to enable mixed-signal design. Core team members include Analogy and Compass Design Automation. In addition, the consortium will be supported by Alternative Systems Concepts, Raytheon, and the University of Cincinnati, all of whom are active in AHDL research. The program will be managed by Rome Laboratory's Willis Horth, who can be reached at (315) 330-2241. *LM*

## NONVOLATILE IC ANALOG MEMORY UPS PERFORMANCE

Nearly three years ago, a silicon chip that could record and play back 16 seconds of better-than-telephone-quality sound was developed using analog EEPROM techniques (ELECTRONIC DESIGN, *Jan. 31, 1991, p. 39)*. Refinements in circuit design and layout, as well as an improved algorithm, have allowed its developer, Information Storage Devices, San Jose Calif., to increase this time to 60 seconds without reducing the original bandwidth of 3.4 kHz (90 seconds is also available in a lower-bandwidth version of 2.3 kHz). The IC's audio specifications were also enhanced—total harmonic distortion was reduced from 1 to 0.5% and the signal-to-noise ratio increased from 35 to 41 dB. Moreover, the chip's price was pared substantially. Other changes include isolating the critical comparator circuit from audio signals to be recorded. The new algorithm accurately adjusts the writing method to the characteristics of the particular nonvolatile memory elements employed, increasing the resolution of the write circuits. For additional information, call (408) 428-1400. *FG*

## E-MAIL HELPS ENGINEERS DO HIGH-LEVEL DESIGN

Engineers can get quick help with their high-level design problems through an innovation that exploits both e-mail and advanced information-retrieval technology. The Solv-It! customer-support system, developed by Synopsys Inc., Mountain View, Calif., consists of a large knowledge base that users access through e-mail to find answers at any time of the day or night. Solv-It! includes more than 1000 articles, with about 200 additional articles expected to be added every month. All articles are indexed and ranked for their relevance to solving users' questions. It also includes information directly from Synopsys' technical staff, such as answers to questions frequently asked of the company's hotline engineers. Excerpts from documentation, application notes, and release notes; bug fixes and workarounds; information on library development; and system-administration issues can all be accessed without delay through the e-mail system. Response time averages between two and five minutes. For more information, call Synopsys at (415) 962-5000. *LM*

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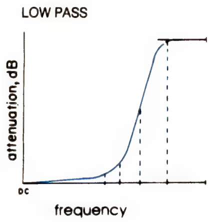

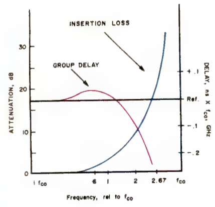

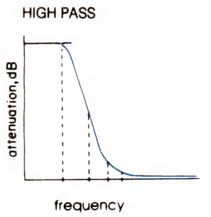

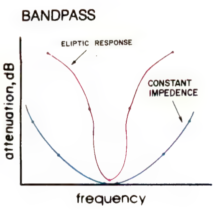

## ***low pass,*** Plug-in, dc to 1200MHz

| Model No. | Passband MHz loss < 1dB | Stopband, MHz loss > 20dB | Stopband, MHz loss > 40dB |
|---|---|---|---|
| ★LP-5 | DC-5 | 8-10 | 10-200 |
| ★LP-10.7 | DC-11 | 19-24 | 24-200 |
| ★LP-21.4 | DC-22 | 32-41 | 41-200 |
| ★LP-30 | DC-32 | 47-61 | 61-200 |
| ★LP-50 | DC-48 | 70-90 | 90-200 |
| ★LP-70 | DC-60 | 90-117 | 117-300 |
| ★P-90 | DC-81 | 121-137 | 167-400 |
| ★LP-100 | DC-98 | 146-189 | 189-400 |
| ★LP-150 | DC-140 | 210-300 | 300-600 |
| ★LP-200 | DC-190 | 290-390 | 390-800 |
| ★LP-250 | DC-225 | 320-400 | 400-1200 |
| ★LP-300 | DC-270 | 410-550 | 550-1200 |
| ★LP-450 | DC-400 | 580-750 | 750-1800 |
| ★LP-550 | DC-520 | 750-920 | 920-2000 |
| ★LP-600 | DC-680 | 840-1120 | 1120-2000 |
| ★LP-750 | DC-700 | 1000-1300 | 1300-2000 |
| ★LP-800 | DC-720 | 1080-1400 | 1400-2000 |
| ★LP-850 | DC-760 | 1100-1400 | 1400-2000 |
| ★LP-1000 | DC-900 | 1340-1750 | 1750-2000 |
| ★LP-1200 | DC-1000 | 1620-2100 | 2100-2500 |

Price, (1-9 qty), all models: plug-in $14.95, BNC $32.95, SMA $34.95, Type N $35.95

### Surface-mount, dc to 570MHz

| | | | |
|---|---|---|---|
| SCLF-21.4 | DC-22 | 32-41 | 41-200 |
| SCLF-30 | DC-30 | 47-61 | 61-200 |
| SCLF-45 | DC-45 | 70-90 | 90-200 |
| SCLF-135 | DC-135 | 210-300 | 300-600 |
| SCLF-190 | DC-190 | 290-390 | 390-800 |
| SCLF-380 | DC-380 | 580-750 | 750-1800 |
| SCLF-420 | DC-420 | 750-920 | 920-2000 |

Price, (1-9 qty), all models: $11.45

### Flat Time Delay, dc to 1870MHz

| Model No. | Passband MHz loss < 1.2dB | Stopband MHz loss > 10dB | Stopband MHz loss > 20dB | VSWR Freq. Range, DC thru 0.2fco X̄ | VSWR Freq. Range, DC thru 0.6fco X̄ | Group Delay Variations, ns Freq. Range, DC thru fco X̄ | Group Delay Variations, ns Freq. Range, DC thru 2fco X̄ | Group Delay Variations, ns Freq. Range, DC thru 2.67fco X̄ |
|---|---|---|---|---|---|---|---|---|
| ★BLP-39 | DC-23 | 78-117 | 117 | 1.3:1 | 2.3:1 | 0.7 | 4.0 | 5.0 |
| ★BLP-117 | DC-65 | 234-312 | 312 | 1.3:1 | 2.4:1 | 0.35 | 1.4 | 1.9 |
| ★BLP-156 | DC-94 | 312-416 | 416 | 0.3:1 | 1.1:1 | 0.3 | 1.1 | 1.5 |
| ★BLP-200 | DC-120 | 400-534 | 534 | 1.6:1 | 1.9:1 | 0.4 | 1.3 | 1.6 |
| ★BLP-300 | DC-180 | 600-801 | 801 | 1.25:1 | 2.2:1 | 0.2 | 0.6 | 0.8 |
| ★BLP-467 | DC-280 | 934-1246 | 1246 | 1.25:1 | 2.2:1 | 0.15 | 0.4 | 0.55 |
| ▲BLP-933 | DC-560 | 1866-2490 | 2490 | 1.3:1 | 2.2:1 | 0.09 | 0.2 | 0.28 |
| ▲BLP-1870 | DC-850 | 3740-6000 | 5000 | 1.45:1 | 2.9:1 | 0.05 | 0.1 | 0.15 |

Price, (1-9 qty), all models: plug-in $19.95, BNC $36.95, SMA $38.95, Type N $39.95
NOTE: ▲: -933 and -1870 only with connectors, at additional $2 above other connector models.

## ***high pass,*** Plug-in, 27.5 to 2200MHz

| Model No. | Stopband MHz loss < 40dB | Stopband MHz loss < 20dB | Passband, MHz loss < 1dB | VSWR Pass-band Typ. |
|---|---|---|---|---|
| ★HP-25 | DC-13 | 13-19 | 27.5-200 | 1.8:1 |
| ★HP-50 | DC-20 | 20-26 | 41-200 | 1.5:1 |
| ★HP-100 | DC-40 | 40-55 | 90-400 | 1.8:1 |
| ★HP-150 | DC-70 | 70-95 | 133-600 | 1.8:1 |
| ★HP-175 | DC-70 | 70-105 | 160-800 | 1.5:1 |
| ★HP-200 | DC-90 | 90-116 | 185-800 | 1.6:1 |
| ★HP-250 | DC-100 | 100-150 | 225-1200 | 1.3:1 |
| ★HP-300 | DC-145 | 145-170 | 290-1200 | 1.7:1 |
| ★HP-400 | DC-210 | 210-290 | 395-1600 | 1.7:1 |
| ★HP-500 | DC-280 | 280-365 | 500-1600 | 1.8:1 |
| ★HP-600 | DC-350 | 350-440 | 600-1600 | 2.0:1 |
| ★HP-700 | DC-400 | 400-520 | 700-1800 | 1.6:1 |
| ★HP-800 | DC-445 | 445-570 | 780-2000 | 2.1:1 |
| ★HP-900 | DC-520 | 520-660 | 910-2100 | 1.8:1 |
| ★HP-1000 | DC-550 | 550-720 | 1000-2200 | 1.9:1 |

Price, (1-9 qty), all models: plug-in $14.95, BNC $36.95, SMA $38.95, Type N $39.95

## ***bandpass,*** Elliptic Response, 10.7 to 70MHz

| Model No. | Center Freq. (MHz) | Passband I.L. 1.5 dB Max. (MHz) | 3 dB Bandwidth Typ. (MHz) | Stopbands I.L. > 20dB at MHz | Stopbands I.L. > 35dB at MHz |
|---|---|---|---|---|---|
| ★BP-10.7 | 10.7 | 9.6-11.5 | 8.9-12.7 | 7.5 & 15 | 0.6 & 50-1000 |
| ★BP-21.4 | 21.4 | 19.2-23.6 | 17.9-25.3 | 15.5 & 29 | 3.0 & 80-1000 |
| ★BP-30 | 30.0 | 27.0-33.0 | 25-35 | 22 & 40 | 3.2 & 99-1000 |
| ★BP-60 | 60.0 | 55.0-67.0 | 49.5-70.5 | 44 & 79 | 4.6 & 190-1000 |
| ★BP-70 | 70.0 | 63.0-77.0 | 68.0-82.0 | 51 & 94 | 6.0 & 193-1000 |

Price, (1-9 qty), all models: plug-in $18.95,
BNC $40.95, SMA $42.95, Type N $43.95

### Constant Impedance, 21.4 to 70MHz

| Model No. | Center Freq. MHz | Passband MHz loss < 1dB | Stopband loss > 20dB at MHz | VSWR 1.3:1 Total Band MHz |
|---|---|---|---|---|
| ★IF-21.4 | 21.4 | 18-25 | 1.3 & 150 | DC-220 |
| ★IF-30 | 30 | 25-35 | 1.9 & 210 | DC-330 |
| ★IF-40 | 42 | 35-49 | 2.6 & 300 | DC-400 |
| ★IF-50 | 50 | 41-58 | 3.1 & 350 | DC-440 |
| ★IF-60 | 60 | 50-70 | 3.8 & 400 | DC-500 |
| ★IF-70 | 70 | 58-82 | 4.4 & 490 | DC-550 |

Price, (1-9 qty), all models: plug-in $14.95,
BNC $36.95, SMA $38.95, Type N $39.95

NOTE: ★**Add Prefix P, B, N, or S for Pin, BNC, N, or SMA connector requirement.**

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## MODELS REPLACE POWER-DEVICE PROTOTYPES

A technology agreement between Analogy Inc., Beaverton, Ore., and Motorola's Semiconductor Products Sector, Phoenix, Ariz., aims to eliminate hardware prototypes of new power components and reduce design-cycle time. Under the terms of the agreement, Analogy and Motorola will jointly develop virtual prototypes (software models) of components that will replace actual hardware samples for customer evaluation. Ultimately, by eliminating an often lengthy prototype-evaluation phase, time to market will be shortened substantially. Motorola will provide proprietary process-technology information, and Analogy will then create the models with its Saber mixed-signal simulator. Analogy's Mast analog hardware-description language is the enabling technology behind the virtual parts. It can accurately model electrical, mechanical, and hydraulic behavior. And because native units are employed rather than electrical equivalents, the models are intuitive and easy to use. In addition, Mast can represent the loads that these power components will drive. The library will ultimately comprise 50 parts ranging from IGBTs and MOSFETs to fluorescent ballast drivers. For more information about the virtual prototypes, call Analogy's Doug Goodman at (503) 626-9700, or Motorola's Lora Blaser at (602) 244-3467. *LM*

## NOVEL GAAS ICS PROPEL PERSONAL COMMUNICATIONS

Designers of personal-communications systems and users of digital logic circuits have much to look forward to judging from the technical program of the upcoming GaAs IC Symposium. Notable developments at the symposium, to be held at the Fairmont Hotel, San Jose, Calif., from Oct. 10 to 13, include a MMIC mixer, based on high-electron-mobility transistors (HEMTs), for 60-GHz indoor communications. The mixer was jointly developed by the Advanced Millimeter Wave Technologies Co. Ltd., and Fujitsu Ltd., both in Kawasaki, Japan. A 0.3-µm AlGaAs HEMT process was used by the Fraunhofer Institute, Erlangen and Freiburg, Germany, to come up with a 3.6-Gsample/s, 5-bit ADC. Rensselaer Polytechnic Institute, Troy, N.Y., in conjunction with IBM Corp., Yorktown Heights, N.Y., designed a 32-bit 400-MIPS monolithic processor fabricated with MESFETs. At the show, Fujitsu Ltd., Tokyo, will unveil a 25,000-gate BDCFL gate array with differential push-pull ECL I/O lines. And International, Newbury Park, Calif., created a heterojunction-bipolar-transistor-based array capable of 5-GHz operation. The conference is sponsored by the Institute of Electrical and Electronic Engineers (IEEE). For registration information, call Harry Kuemmerle III at (310) 459-4691; or fax at (310) 459-0605. *DB*

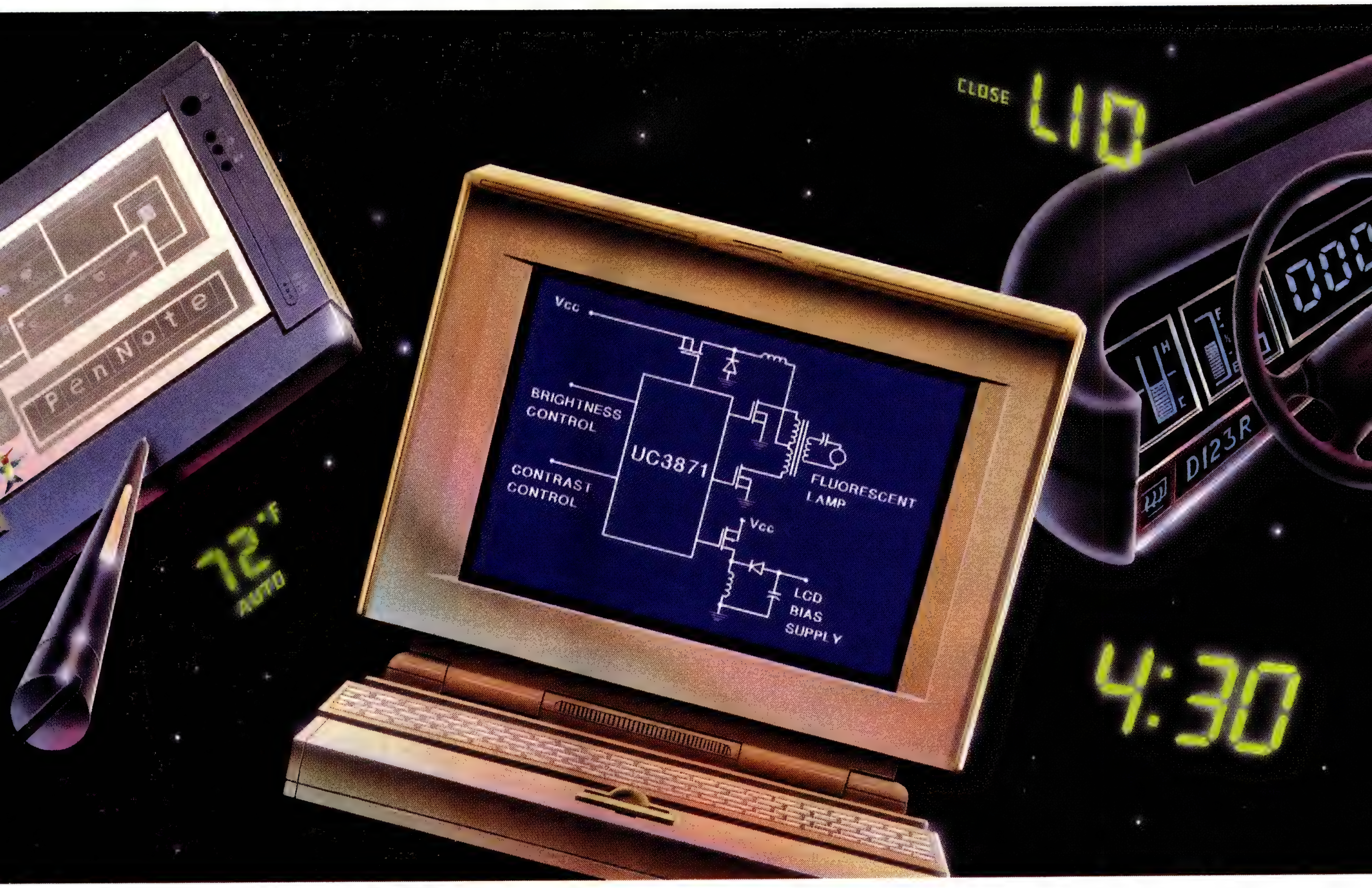
## TOOLKIT TARGETS MCS-96 EMBEDDED TASKS

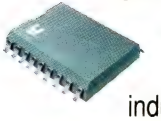
Embedded and real-time development for Intel's MCS-96 microcontrollers stands to get a boost thanks to a new ANSI C compiler toolkit. The kit's developer, BSO/Tasking, Dedham, Mass., licensed source code for the controller's software development tools from Intel Corp., Santa Clara, Calif., and integrated it with its own in-circuit emulation and real-time operating system products. Besides NT and NQ 20-bit extended derivatives and an ANSI C compiler, the MCS-96 toolkit has a macro assembler, locating linker, librarian, extended floating-point library, and other utilities for a DOS environment. The kit supports Intel's ApBuilder and ProjectBuilder. Ports to Unix are expected next year. For more information, call BSO/Tasking at (617) 320-9400. *SVT*

## AGREEMENT SPURS ZINC-AIR BATTERY DEVELOPMENT

A licensing agreement between AER Energy Resources Inc., Smyrna, Ga., and Westinghouse Electric Corp., will accelerate the development of long-running and rechargeable zinc-air batteries, potentially doubling or even quadrupling the run time of portable computers. Run times for portable notebook and pen-based computers of 8 hours or more are being pursued by AER. The agreement is exclusive for portable computers and non-exclusive for all other portable products. The proprietary technology licensed from Westinghouse—an air cathode that absorbs oxygen from air to generate electrical current on battery discharge and expels oxygen during battery recharge—allows the batteries to achieve a high energy-density-to-weight ratio. This is partly due to the fact that zinc-air batteries don't require a heavy metal electrode like nickel or lead. The technology was originally developed at Westinghouse's Science and Technology Center, Youngwood, Pa. This past August, AER began manufacturing zinc-air batteries and is currently sampling them with four OEM computer manufacturers. For more information, contact Frank Harris at AER at (404) 433-2127. *DM*

# Light Years Ahead





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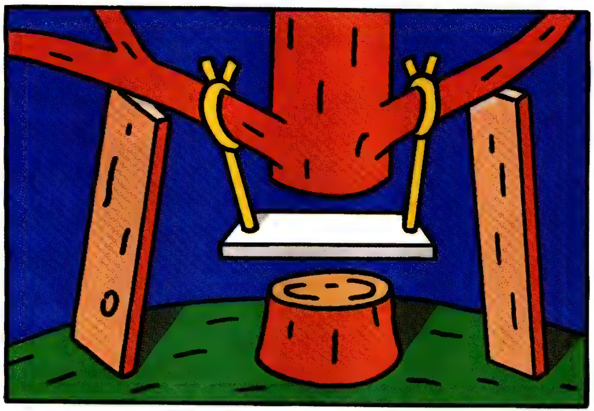
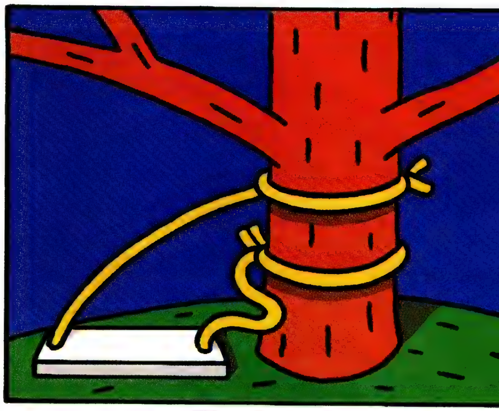
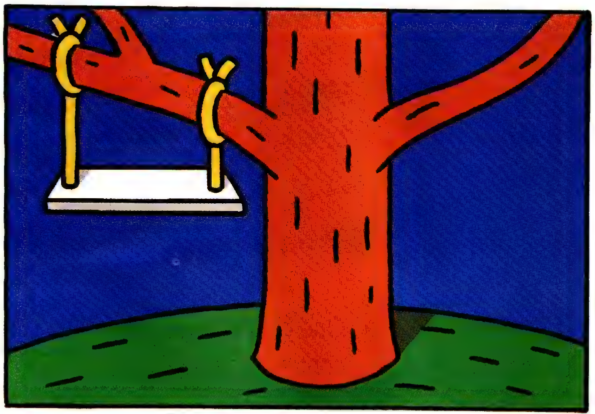
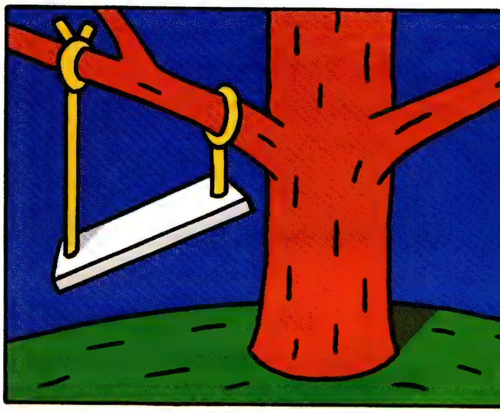
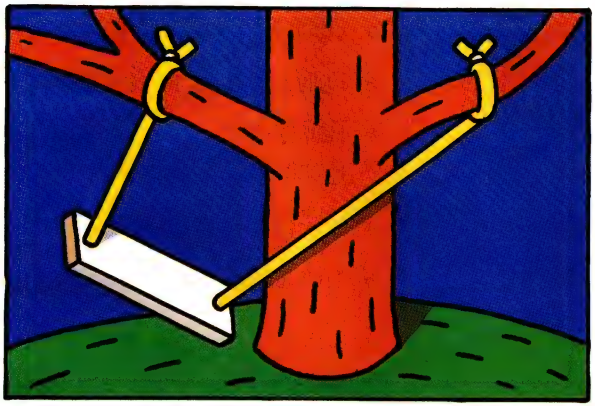
# Xilinx FPGAs. The perfect parts for an imperfect world.

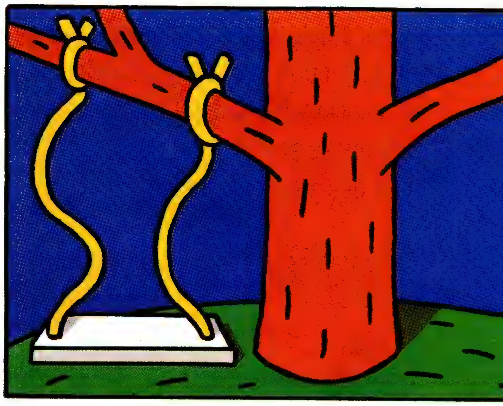

*What Marketing Asked For*


*What Design Specified*


*How Manufacturing Built It*


*What QA Approved*


*What Engineering Developed*


*What Documentation Described*

Look familiar?

We're willing to bet a sizable chunk of next week's pay that a cartoon like this hangs in just about every engineering department in this country.

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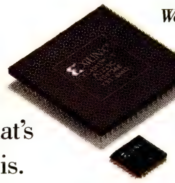

*We have as many options as you need (more than 350, in fact), from our new 13,000 gate XC4013 FPGA, to our space-saving TQFP.*

why not choose a logic device that won't let you go wrong?

Nothing does that better than an FPGA from Xilinx.

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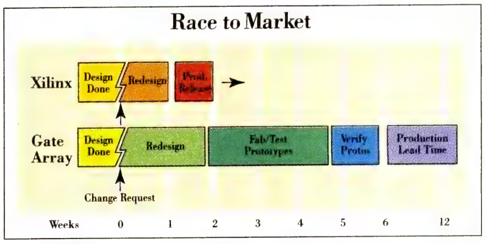

*With FPGAs from Xilinx, you can get to market faster even if you make a ton of changes — all in less time than a single gate array change cycle.*

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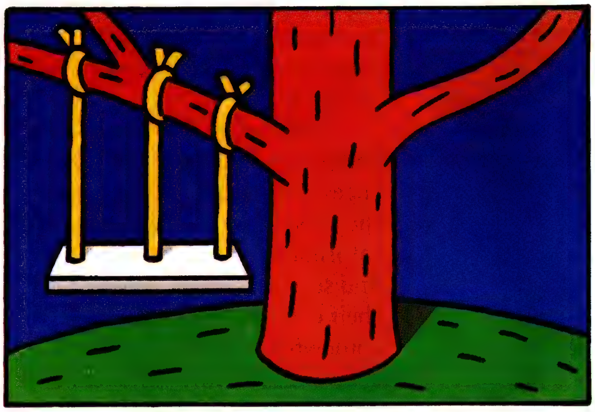
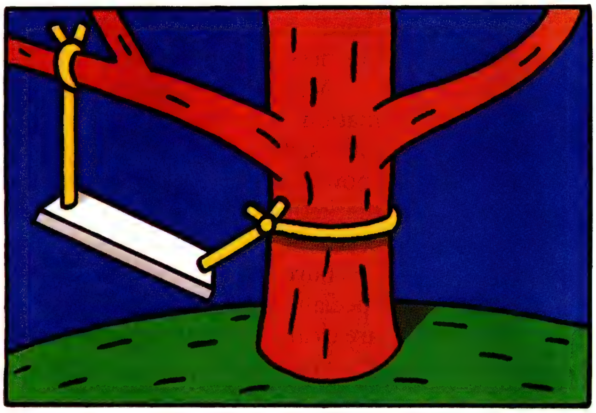
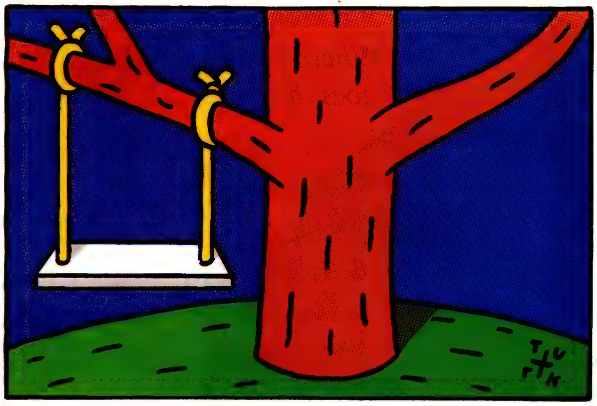


*What Management Agreed On*



*How Marketing Changed It*



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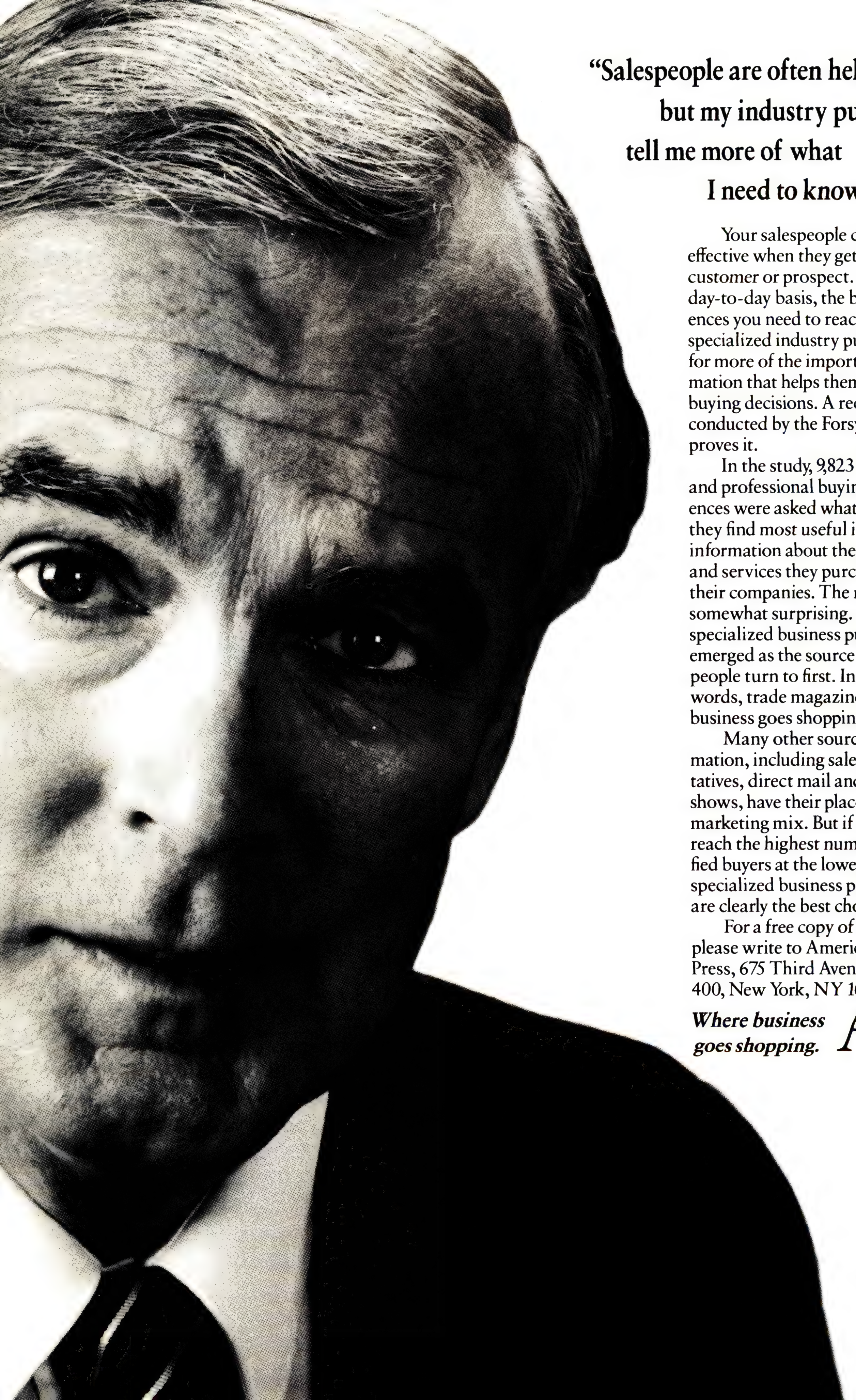
CIRCLE 127 FOR U.S. RESPONSE

CIRCLE 128 FOR RESPONSE OUTSIDE THE U.S.



# “Salespeople are often helpful, but my industry publications tell me more of what I need to know.”

Your salespeople can be effective when they get to see a customer or prospect. But, on a day-to-day basis, the buying influences you need to reach turn to specialized industry publications for more of the important information that helps them make buying decisions. A recent study, conducted by the Forsyth Group, proves it.

In the study, 9,823 business and professional buying influences were asked what sources they find most useful in providing information about the products and services they purchase for their companies. The results were somewhat surprising. Overall, specialized business publications emerged as the source business people turn to first. In other words, trade magazines are where business goes shopping.

Many other sources of information, including sales representatives, direct mail and trade shows, have their place in the total marketing mix. But if you want to reach the highest number of qualified buyers at the lowest cost, specialized business publications are clearly the best choice.

For a free copy of the study, please write to American Business Press, 675 Third Avenue, Suite 400, New York, NY 10017.

***Where business goes shopping.*** **ABP**

# FINE-GRAIN FPGA ARCHITECTURE USES FOUR LEVELS OF CONFIGURATION HIERARCHY

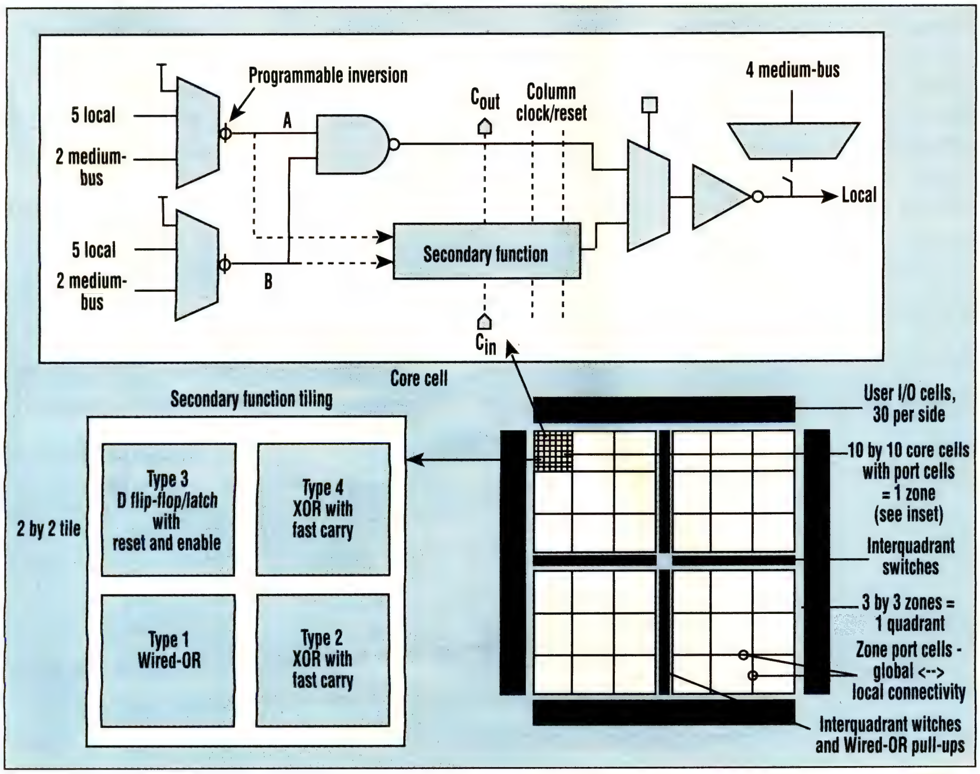
The battle between coarse - grained SRAM-based field-programmable gate arrays and one-time-programmable fine-grained FPGAs may soon be over. A new fine-grained tiled architecture achieves leading-edge performance and high logic density thanks to a novel hierarchical-routing structure.

The SRAM-based architecture will feature the best capabilities of both the fine- and coarse-grain approaches. Jointly developed by Motorola Inc., Phoenix, Ariz., and Pilkington Microelectronics Ltd., Cambridge, England, it sets up four granularity levels resembling checkerboards within checkerboards *(see the figure)*.

In the first family member in the MPA10X series, the MPA1036, the array's highest level is designed as four quadrants separated by interconnection matrices (intraquadrant switches) and surrounded by I/O cells. Each quadrant is further subdivided into nine zones, and each zone contains a 10-by-10 array of fine-grain logic cells surrounded by port interface cells. Port cells provide programmable connections between zones, plus programmable connections from the intrazone routing to the global buses.

All logic cells can be programmed to function as an AND gate. However, the cells are actually grouped into 2-by-2 tiles, with each cell in the tile also possessing a second configuration state *(see inset to figure)*. Thus, each tile either has four AND gates, four alternative logic cell types, or any combination thereof. Two of the cells can be exclusive-OR (XOR) elements with fast-carry circuits (cell positions 2 and 4, referred to as types 2 and 4), while one of the cells is a Wired-OR driver (tile position 1, or type 1) that can be used to create Wired-OR buses within each zone. The fourth cell can be a D flip-flop or latch with Reset and Enable lines (tile position 3, or type 3).

The fine granularity coupled with a high-performance 0.65-μm CMOS process results in functions such as a three-level NAND delivering a delay of between 2.8 to 3.7 ns, depending on the array's speed grade. Global bus delays are typically between 2 and 3 ns, with the longest corner-to-corner delay being 8 to 10 ns. The sequential elements have a setup time of only 1.2 ns and a clock-to-output time of 1.5 ns, allowing the flip-flops to toggle at over 200 MHz.


Programmable inversion
5 local
2 medium-bus
A
5 local
2 medium-bus
B
$C_{out}$
Column clock/reset
Secondary function
$C_{in}$
4 medium-bus
Local
Core cell
Secondary function tiling
2 by 2 tile
Type 3 D flip-flop/latch with reset and enable
Type 4 XOR with fast carry
Type 1 Wired-OR
Type 2 XOR with fast carry
User I/O cells, 30 per side
10 by 10 core cells with port cells = 1 zone (see inset)
Interquadrant switches
3 by 3 zones = 1 quadrant
Zone port cells - global <--> local connectivity
Interquadrant witches and Wired-OR pull-ups

Preliminary tests indicate that the FPGAs will operate with 70-MHz system clocks, even with the chip's logic fully utilized.

There are four levels of interconnection. Device-level interconnects tie the quadrants together and quadrant-level interconnects tie the zones within a quadrant together. Zone-level interconnects are used within a zone to tie the cells together (medium buses or M-buses) and local-level interconnects tie each core cell to eight of its neighbor cells. Each zone contains four M-buses in every row and column in the zone.

Such a routing hierarchy optimizes circuit performance at each interconnection level. The scheme also reduces interconnection options at the core-cell level, shrinking the cell and allowing more cells to be integrated on a chip. The first version, the MPA1036, has 3600 core cells. The MPA1064 and 1100 versions will offer 6400 and 10,000 core cells, respectively.

Each core cell holds two input multiplexers, and each multiplexer has seven input signals, any one of which can be selected. Five of the sources come from the local level and two from the zone-level interconnections. Each core cell's output can be connected to as many as eight other core cells using local interconnections. That local interconnection allows multiple core cells to be grouped together to form more complex elements, such as full adders, 2-input multiplexers, T or J-K flip-flops, etc.

In addition, the output can be routed to four zone-level buses. Moreover, if the cell isn't driving a zone-level bus, the cell can be used to join a horizontal and a vertical bus together to turn a signal path by 90°. Core cells also have other uses—they can be used to rebuffer a signal or provide additional routing. As a result, each core cell actually has three states: It either serves its primary function (AND gate), its secondary function (XOR, wired-OR, or D flip-flop), or as a repowering buffer. All core cells can also invert the inputs, or perform a 2-input AND function with programmable input inversion.

The I/O cells that surround each quadrant are set up in such a way where there's one I/O cell for every two rows or columns of logic cells. That, for instance, gives the MPA1036 a total of 120 I/O pins. Each I/O cell has input and output registers and can be individually programmed to support 3- or 5-V logic levels as well as CMOS or TTL levels. The cells supply drive strengths of 6, 12, or 24 mA. An 8-bit bus is also included in the periphery between the array and the I/O cells. In addition, JTAG boundary-scan testing can be implemented with minimal overheads.

To maximize the performance of circuits configured in the fine-grained architecture, Motorola teamed with NeoCAD Inc., Boulder, Colo., to develop timing-driven design tools that run under NeoCAD's Foundry toolset. The tools incorporate both timing- and frequency-driven automatic place-and-route capability, as well as a full-featured graphical manual editor. An extensive library of simple logic cells and complex macrocells is under development.

*DAVE BURSKY*

# PLUG-AND-PLAY STANDARD AIMS TOWARD SELF-CONFIGURING PCs

Tracking down an interrupt, a DMA channel, or some other control-line conflict when installing a new card in an IBM PC or compatible usually can become a protracted and tedious ordeal. For users who have spent long hours on such tasks, the recently approved "Plug and Play" standard is a welcome sight.

In retrospect, the new standard, developed by Microsoft Corp., Redmond, Wash., and many other chip and system suppliers, probably defines what the PC and all add-in cards should have done from the start. Basically, the system should be able to determine all of the resources; set up the proper non-conflicting addresses, interrupt lines, DMA channels, and other operation aspects for each function; and then load in the appropriate drivers for each function.

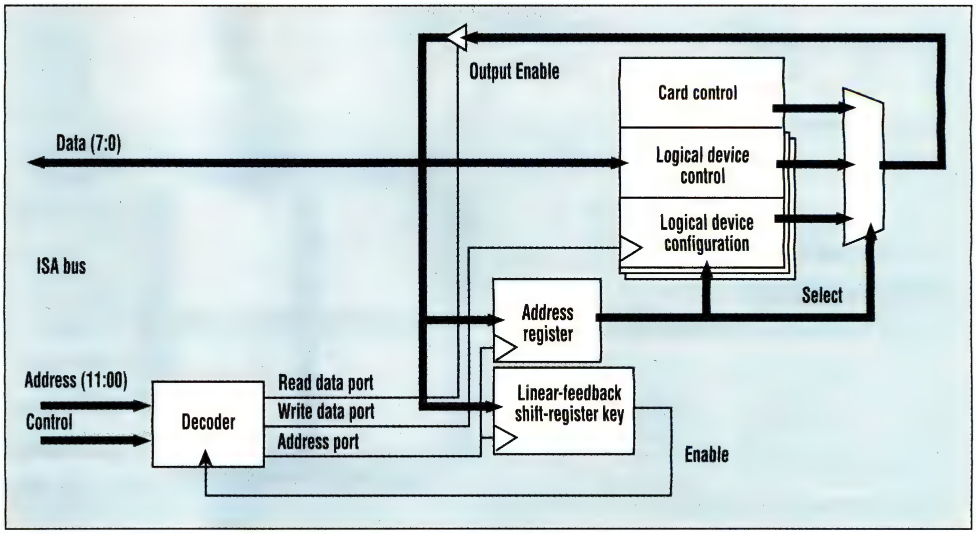
The new standard is bus-independent, and will thus be applicable to the ISA, EISA, MicroChannel, PCMCIA, and other "buses" used within personal computers (the bidirectional parallel port, for instance). However, Plug and Play first will be implemented for the ISA bus. That bus was selected due to its pervasiveness—there are close to 100 million ISA-based systems already in use and close to 30 million more per year entering the user base.

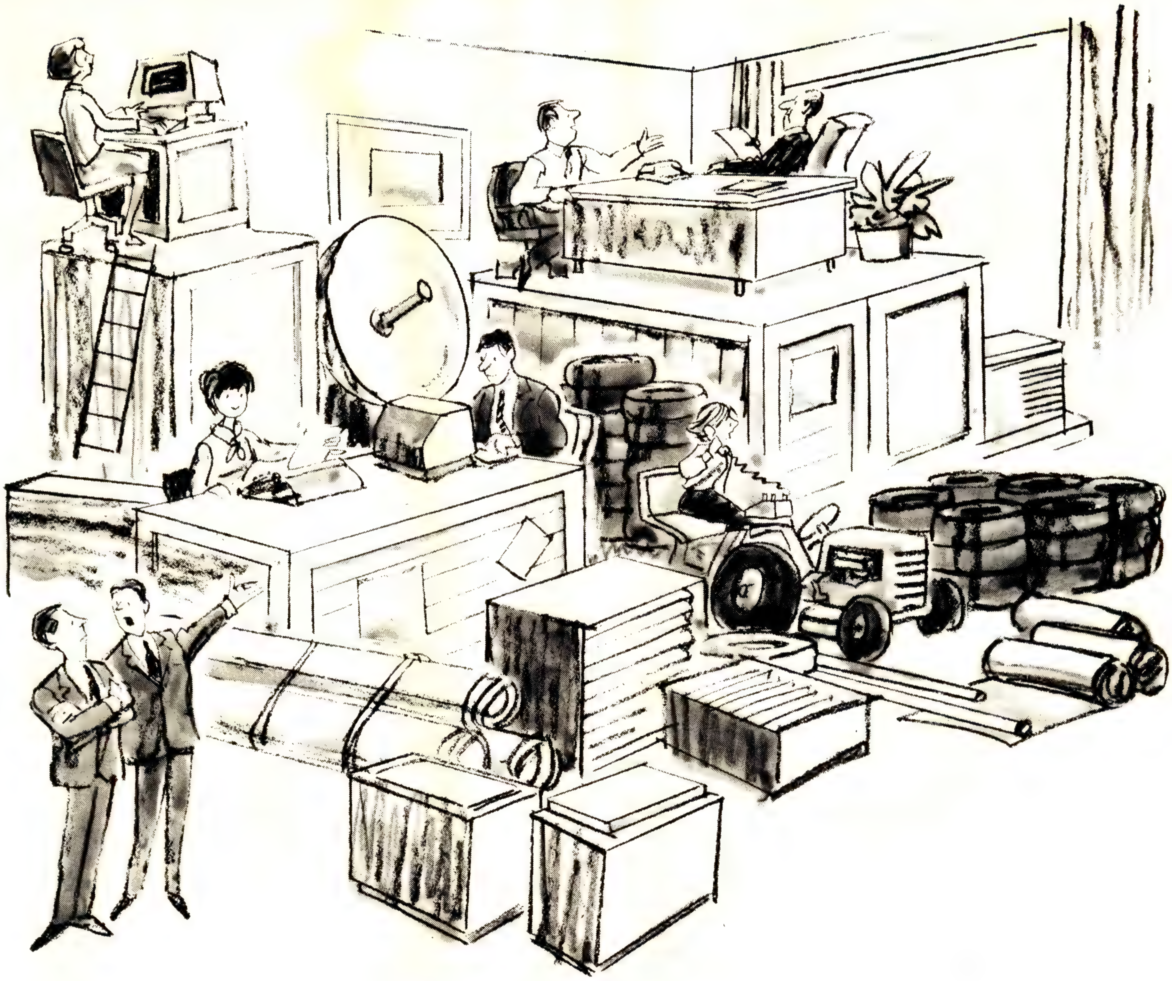
Cards and systems based on the EISA, MCA, and PCI buses have developed some degree of self-identification, so the Plug and Play standard will address those buses in future releases. Furthermore, a form of Plug and Play standard already exists for PCMCIA interfaces. Some card makers haven't followed it fully, though, creating a credibility gap the Personal Computer Memory Card Industry Association hopes to resolve in the future.

The jointly developed Plug and Play standard eliminates the "plug and pray" problem for nontechnical users. It also trims to near zero the time needed to configure or reconfigure a system for the knowledgeable user. Most existing ISA systems can probably be upgraded by updating the operating system or BIOS (or both) and substituting Plug-and-Play-compatible add-in cards for the existing ISA add-in cards. However, most such systems won't ever see an upgrade.

Prime candidates for the Plug and Play upgrade include newer systems that employ a flash-memory-based BIOS or those expected to be upgraded for multimedia capabilities. Of course, newly built ISA-based systems and portables slated for introduction late this year and beyond will be incorporating the Plug and Play upgrade directly in the BIOS and operating system. These systems will be able to tell the user not only what resources are available on the motherboard, but also what cards are plugged into the ISA or other expansion buses. Microsoft's forthcoming "Chicago" version of its Windows operating system has a bus enumerator that displays system configuration.

The basic functions per-





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formed in the Plug and Play standard consist of four steps: isolate the ISA card, read the card's resource data, identify the card and configure its resources, and locate a driver for the card. The flexibility of the standard allows a card to start up as either active or inactive. Each card can be configured by the system with the knowledge of what resources were allocated for the other cards. Therefore, multiple and identical cards can be plugged into a system and still operate independently.

In a demonstration by Microsoft, two Plug-and-Play-compatible audio cards were inserted into a Plug and Play system (a current PC running a beta version of Chicago), the system was booted, and each card was assigned different interrupts and drivers through the operating system. Consequently, both cards operated and produced independent and simultaneous audio-output signals.

Information stored on the card that's read by the host system provides such details as memory and I/O space, DMA channels, and interrupt levels supported. A typical autoconfigurable interface consists of an 8-bit register set to retain the configuration data, an address register, and some nonvolatile memory space to hold a unique identifier (a 72-bit, unique, non-zero number composed of two 32-bit fields and an 8-bit checksum) and resource information *(see the figure).*

The host software automatically analyzes the contents at every hard system reset. Older ISA cards that are intermixed with Plug and Play cards will interoperate. However, those older cards must still be manually configured. To isolate a card during the configuration sequence, the mechanism depends on the unique number stored in each card. The number provides an identifier that allows the host to select each card in turn. The number contains a 32-bit vendor-identifier field, a 32-bit arbitrary-number field, and the 8-bit checksum. Combining those fields provides a unique number, thus no two cards in a system will have the same identifier.

After the card is isolated, the Plug and Play software assigns each card a "handle," which is used to select that unique card. Handles eliminate the need for the system to use a more elaborate and more time-consuming isolation protocol. After isolating the cards and assigning the handles, the cards are read over three 8-bit ports, the resource information from all of the cards is analyzed, and the resources are arbitrated and allocated.

Card configuration is done by control bits sent by the host to command registers on each card. In some cases, certain resources may not be reconfigurable. When this occurs, the card informs the arbiter that it can't assign the requested resources. After all resources are allocated, the operating system can invoke an I/O-conflict-detection routine to ensure that assigned I/O resources aren't conflicting with non-Plug-and-Play cards.

For more information, contact Moshe Lichtman at (206) 936-7292. You can also sign on to the Plug and Play forum on Compuserve (go plugplay) to obtain a copy of the standard.

*DAVE BURSKY*

# LASER SCANNING CAPTURES WHITEBOARD IMAGES

A novel laser-scanning scheme will forever change the look of conference-room electronic whiteboards. It not only captures writing and drawings, but also displays images in up to four colors on computer monitors as well as on the whiteboard. Developed by Microfield Graphics Inc., Beaverton, Ore., the scanning scheme captures the movement of the specially marked pens or erasers on a hard-surface whiteboard. This eliminates the need for the pressure-sensitive whiteboards that can't recognize erasures or colors and suffer from reliability problems.

The Softboard system employs two invisible infrared (IR) laser beams, each located in one of the upper corners of the 60-in.-wide-by-54-in.-high whiteboard. The beams continuously scan the entire area of the whiteboard, about 0.25-in. above the board's surface. Marking pens or erasers used to write on the board are configured with bar-code rings. These rings identify what they are and their color. When a user writes with these implements, the laser scanners capture the bar-code and position information.

The data capture takes place in real time: Data is interpreted by a single TMS320C26 DSP IC running at 40 MHz, and then forwarded in greatly compressed form over an RS-232 data link (typically running at 4800 baud) to a host. The laser scanners are built from standard 780-nm IR laser modules, multifaceted scanner mirrors, and returned-IR-light collection and detection assemblies.

The emitting beams from the scanners sweep across the board surface. When they come in contact with a marker or eraser, the reflected beams are collected on its return paths off the scanner mirror and focused on the respective photodiodes.

The modulated light being returned contains all of the necessary information about the marker's or eraser's relative position, motion, and type (the use of encoded retro-reflectors is one of the key patent-pending aspects of the system). By gathering information from the two scanners at the same time, the exact position of the pen or eraser can be tracked anywhere on the writing surface by triangulation.

When connected to a PC or Macintosh computer via the serial port, the Softboard sends all captured information to the computer's display. Computers with color displays can display images in four colors (black, red, green, and blue, for example). Each screen can then be saved to a computer file and either printed or faxed. It could also be transmitted to another site over a modem.

In fact, with a modem link and a telephone, bidirectional meetings could be held. With Softboards and computers at each location, images can be transferred back and forth in real time without tedious transcriptions.

The Softboard is slated for delivery next month. Contact Pete Zinsli at (503) 626-9393.

*DAVE BURSKY*

New Release
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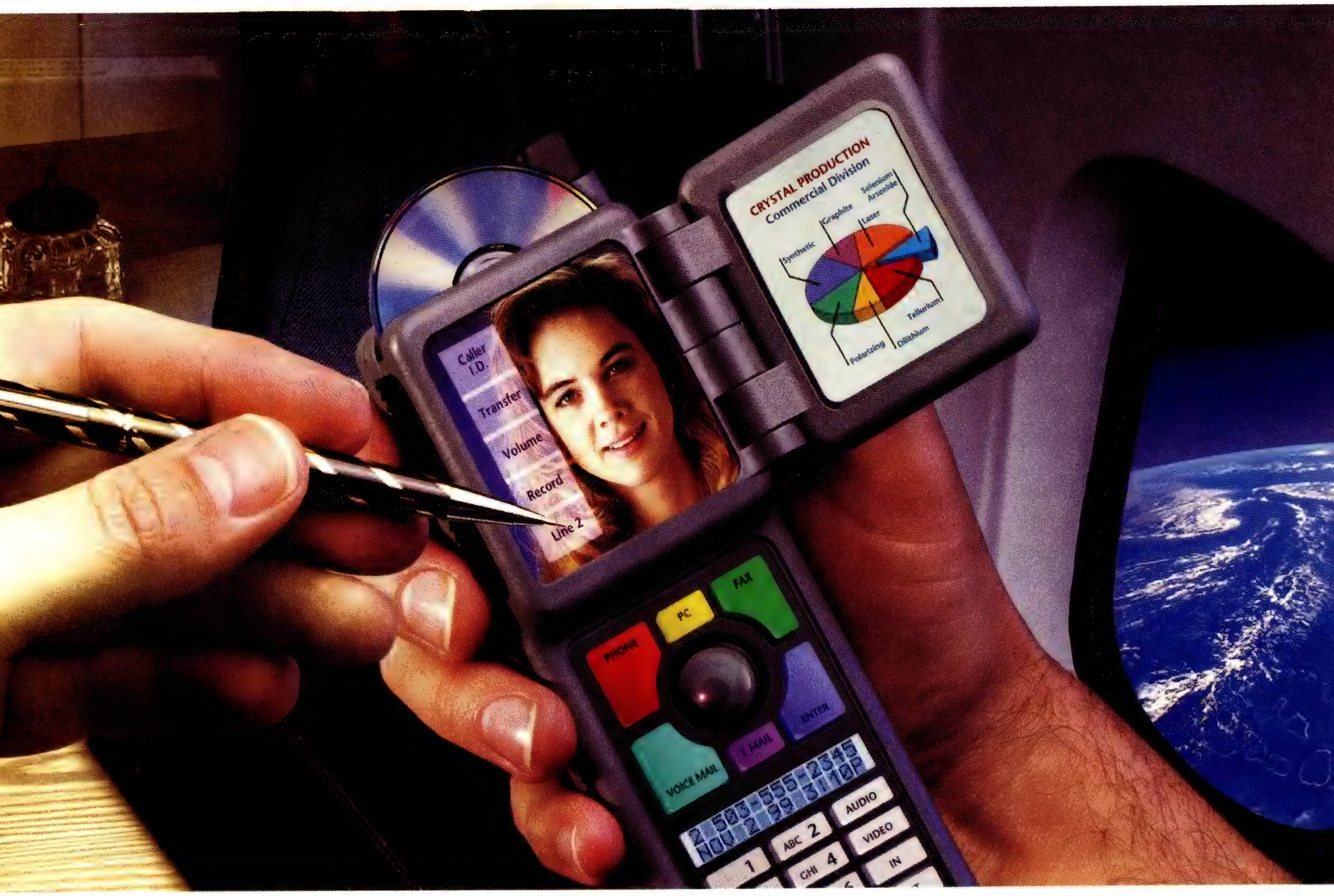

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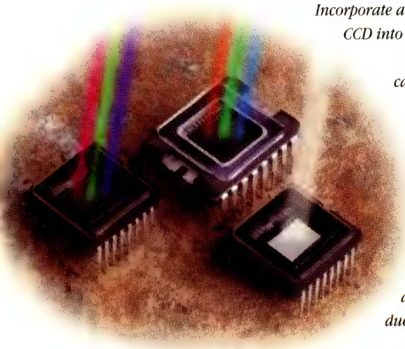

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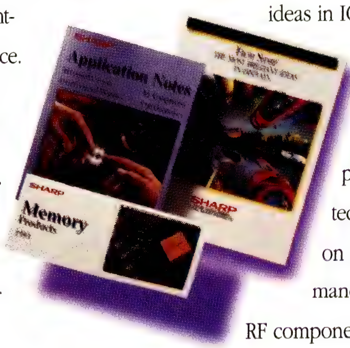

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# SERVICE GROUPS HELP USERS EXPLOIT EDA TECHNOLOGY

## ENGINEERS LOOK TO OUTSIDE SOURCES TO SQUEEZE PRODUCTIVITY FROM LEADING-EDGE DESIGN ENVIRONMENTS.

**LISA MALINIAK**

You don't need to know a lot about personal computers to realize their productivity potential. But what's usually not anticipated is the learning curve associated with any new technology. For instance, John Q. Public recognizes that a PC would help him to organize his files, calculate his taxes, better handle his finances, and so on. He takes the step of investing in the computer and associated software, but then finds himself staring at the screen, unable to tap into the reservoir of productivity he longed for.

Similar situations are occurring today in the world of electronic design automation (EDA). Design teams faced with harsh time-to-market pressures are drawn to the lofty promises of leading-edge EDA technology like system simulation, hardware-description languages, logic synthesis, and top-down design. Unfortunately, although the designers know which technology they need, they often lack the time and manpower to implement it.

The good news is that designers can get help. EDA vendors are hearkening the cry of designers by establishing service divisions that aren't dedicated to selling tools, but rather to implementing new design methodologies, and making existing design environments more productive. Leading-edge companies like Cadence Design Systems, Mentor Graphics, Synopsys, and Zycad all have employees that work with design teams to help them create the EDA environment best suited to their needs.

### A VARIETY OF CHOICES

The types of EDA services that are offered vary widely, including everything from basic software training to complete design methodology implementation. Zycad's Protocol Services Div., Rockaway, N.J., for example, describes their offerings in terms of addressing three user questions: What should I do and how should I do it? Can you help me get it done? And, can you help me put it into practice?

EDA vendors have always offered training for their own software, but they've just recently expanded into process and methodology training. That's because many of the new methodologies require not just tools, but a whole new way of thinking about design. Tools by themselves don't solve problems, but instead are facilitators to problem solving. Jo Anne Karns, vice president of marketing for Protocol, explains that product-development results are a function of tools, methodology, development skills, human resources, and capital resources. At the leading edge, tools alone are insufficient to get the job done.

For instance, Mentor Graphics Corp., Wilsonville, Ore., has been upgrading their services division since 1981. The most basic level of service is customer support in the form of hotlines, bug fixing, and software updates. Most EDA vendors offer this type of service.

The next level is what Mentor terms professional services. These are aimed at getting customers more efficient and shortening their time to market. In such situations, the customers ask for help because they need to get a project done and their tools are falling short. The services group will look at the design process, gather information, and assess what needs to be done using benchmark profiles of what existing customers in similar situations have accomplished. Process assessments are then fed back to the customer's management, along with recommendations for changes. And for the most part, these professional services are tool independent.

Design teams can also contract with the Mentor services group to create integrated environments consisting of Mentor, third-party, and internal tools. For instance, Mentor worked with Hewlett-Packard to create a unified environment composed of Mentor, GenRad, and Verilog software, as well as HP's own design library. After creating the environment, the services group then trained the HP divisions on how to use it. In addition, Mentor will contract to supply parts data, such as libraries and electronic data books. The final type of service they offer is helping engineers switch from one design environment to another.

Cadence Design Systems Inc., San Jose, Calif., also offers various service levels. The first is the traditional tool-oriented services like integration and installation support. Another type of service is methodology consulting. With methodology consulting, the company attempts to answer three user questions: How am I doing? How can I improve my overall design process? And, how can I best manage my assets? Answering these questions gives users perspective when compared with similar design teams, and also helps them exploit their existing design-automation technology.

Design teams can also get help for people-motivation problems. For example, companies may purchase exceptional tools, but then they have trouble getting their design teams to adopt them. Cadence refers to this level of service as "change management" because a company first buys tools, then needs to change the way people behave. According to Bob Leach, the company's senior vice president of consulting and services, this is an area that needs attention because the entire design community has done a poor job of addressing change management.

Zycad Corp.'s service division is a separate company called Protocol. Protocol has consulting, engineering, and process-management services. The consulting service is divided into two phases: assessment and recommendation, and implementation planning. These services include top-down design, system simulation, and design for test. Protocol's engineering services incorporate both packaged and custom engineering, which may entail model development, fault-vector development and verification, and simulation services. Finally, the process-management services may include custom work, such as developing customer partnerships to manage a key part of their development projects.

**Tools and services will always be closely linked and will continually affect each other. In other words, design software can incorporate the knowledge gained by service consultants.**

Moreover, process-management solutions may manage requirements from definition through test. They may also manage the VHDL modeling and simulation acceleration in a major system-integration project.

Synopsys Inc., Mountain View, Calif., has a customer services division that helps users create and use its high-level design automation. Support ranges from initial product installation and training to ongoing support and project-specific consulting services. They have recently expanded their services division to include the industry's first e-mail-based help system.

Many of the smaller, point-tool companies are also entering the EDA service area. For instance, Silvar-Lisco, Sunnyvale, Calif., develops tools for IC layout. Last May, they announced the establishment of a center that supplies design services, integration services, and design-methodology consulting.

All of the recent activity surrounding EDA services suggests how outside help is becoming increasingly important to design teams. Cadence's Bob Leach suggests that in the future, the demand for more services will cause a tiering of the industry. In other words, a two-tier development will result in some companies acting as solution providers, while other companies will be point-tool suppliers.

But the two areas—tools and services—will always be closely linked. Phil Robinson, vice president and general manager of Mentor Graphics' Value Added Services group, explains that tools and services will continually affect each other. For example, service consultants will provide good feedback for tool development. In other words, electronic-design-automation software can incorporate the knowledge gained by consulting services.

Furthermore, standards will affect the future of the services available to design teams. In fact, both design-tool and workstation standards are key to making integrated leading-edge environments less expensive and more accessible.☐

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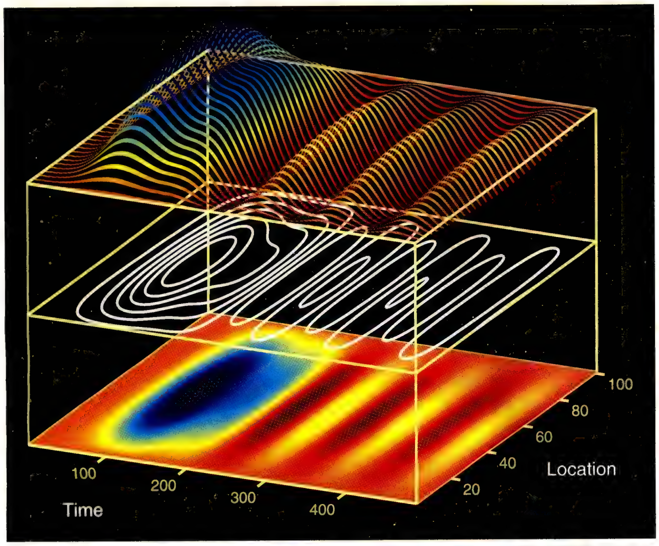

*Three views of bending forces on a magnetic levitation train guideway. Analysis was one part of an 80th-order differential equation modeled with MATLAB. Data courtesy of Grumman Corp.*

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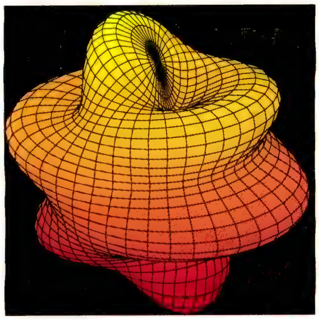

*Visualization of a spherical harmonic function, created with the new Symbolic Math Toolbox.*

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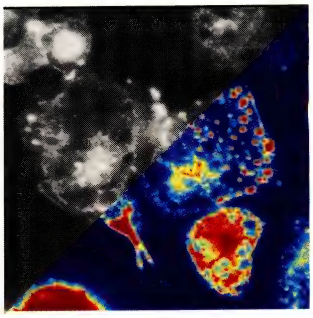

*Enhancement of a cell micrograph using density slicing with the new Image Processing Toolbox.*

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## COMPLETE AUDIO SUBSYSTEM ON A CHIP INTEGRATES DSP CORE, PROGRAMMABLE PHASE-LOCKED-LOOP, CLOCK MULTIPLIER, AND STEREO DAC CIRCUITS.

# IC AIMS AT DIGITAL-AUDIO DECOMPRESSION STANDARDS

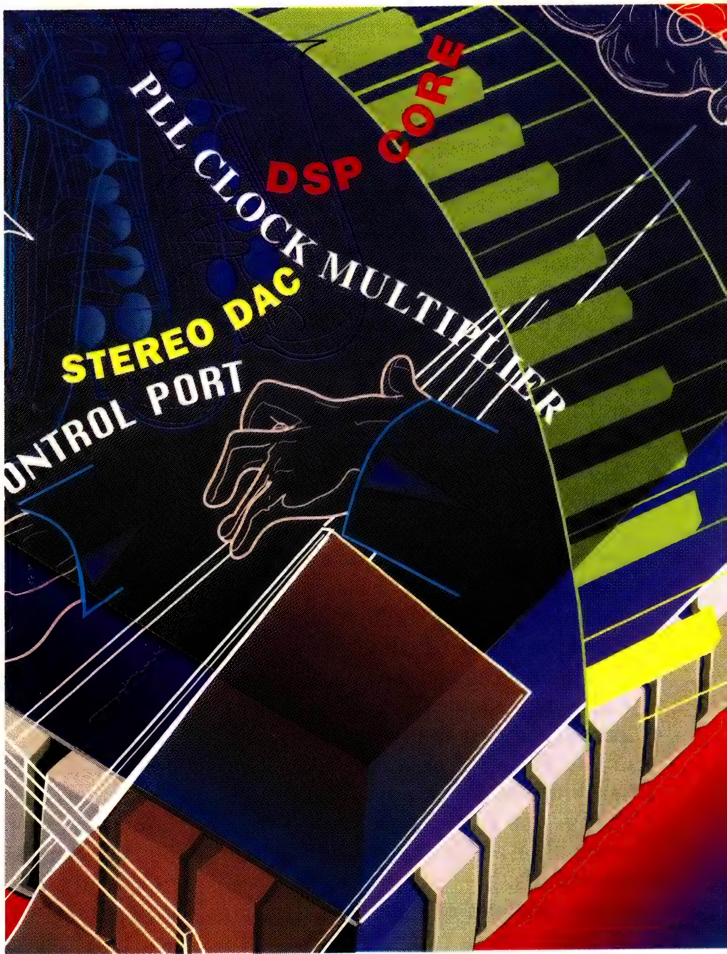
### JACK SHANDLE

It's a widely accepted premise among those in the electronics industry that the mostly digital world of computers and the mostly analog world of consumer products are beginning to merge. Yet there continues to be a great deal of confusion about which standard or standards will still be around when the dust settles a few years from now.

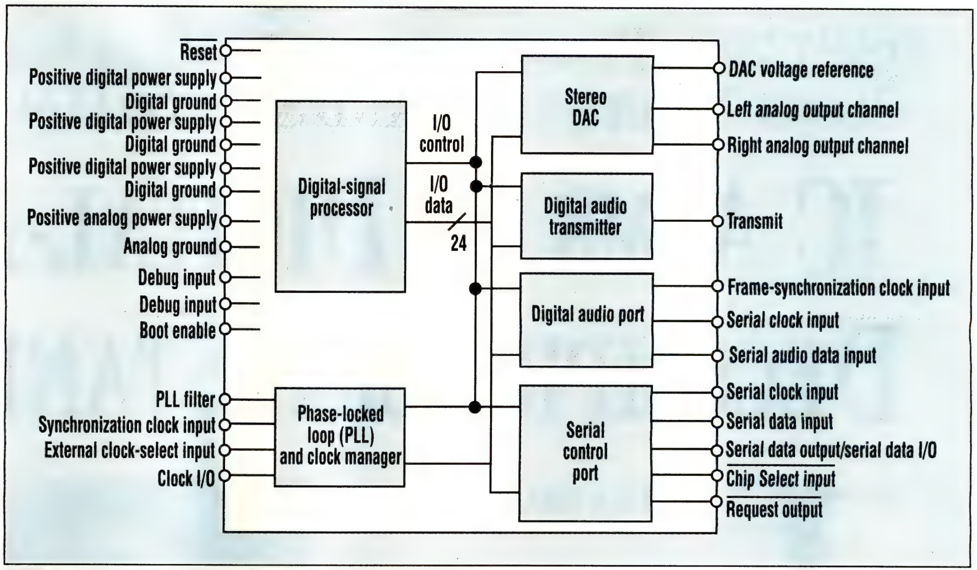
Nowhere is this uncertainty more evident than in the digital-audio arena. The demand for higher-quality sound emanating from speakers has meant a general trend toward digital coding, and more recently, a quest for compression schemes that deliver high-quality sound over relatively narrow bandwidths. CD-ROM applications will clearly benefit by adopting compression because the storage capacity of the disk is limited. But broadcast audio and cable TV also have bandwidth limitations that make compression worthwhile.

From a system designer's point of view, choosing an audio coding technology is a little like betting on a horse—there's always some risk regardless of how much research is done. In handicapping audio compression/decompression, the three prominent contenders are Dolby Laboratories Inc., San Francisco, Calif.; Scientific Atlanta Inc., Norcross, Ga.; and the Motion Picture Experts Group (MPEG) of the International Standards Organization (ISO). All have devised algorithms that provide about 4:1 compression but deliver CD-quality sound. Moreover, the players aren't resting on their laurels. They're busy revising and upgrading their coding techniques on a regular basis, so instead of a three-horse field, it's more like 10 or 12.

Another important factor in the system designer's decision matrix is the semiconductor products that are available to execute the algorithms. To date, the market has seen hardwired solutions such as Texas Instruments Inc.'s TMS320AV110, which implements levels 1 and 2 of the MPEG standard (ELECTRONIC DESIGN, *May 27, p. 139)*. At the other end of the spectrum are general-purpose digital-signal-processor solutions. Motorola Inc.'s 56000 has leveraged its 24-bit data-path architecture to grab hold of most of the high-end audio solutions.



But the generic problems with hardwired and general-purpose solutions are well


Reset
Positive digital power supply
Digital ground
Positive digital power supply
Digital ground
Positive digital power supply
Digital ground
Positive analog power supply
Analog ground
Debug input
Debug input
Boot enable
PLL filter
Synchronization clock input
External clock-select input
Clock I/O
Digital-signal processor
Phase-locked loop (PLL) and clock manager
I/O control
I/O data
24
Stereo DAC
Digital audio transmitter
Digital audio port
Serial control port
DAC voltage reference
Left analog output channel
Right analog output channel
Transmit
Frame-synchronization clock input
Serial clock input
Serial audio data input
Serial clock input
Serial data input
Serial data output/serial data I/O
Chip Select input
Request output

**1. THE FIRST AUDIO SUBSYSTEM** on a chip to decode digital audio data that's compressed by various algorithms is the CS4920 developed by Crystal Semiconductor. Besides its programmable DSP core, the chip integrates stereo DAC capable of CD-quality sound, a clock manager, and other peripherals that have previously required external circuits.

known: The hardwired ICs handle just one algorithm and the general-purpose ICs require additional chips for *specific* solutions. To implement an audio decoding function, for example, the 56000 would require 24-bit-wide SRAM, DACs, and at least one phase-locked-loop (PLL) circuit.

It was only a matter of time before a technologically nimble semiconductor company provided a middle ground. It comes in the form of a programmable DSP core and the associated circuits to implement a complete audio subsystem on a chip. Crystal Semiconductor Corp., Austin, Texas, leveraged its unique ability to do analog functions in digital CMOS to accomplish that goal. The CS4920 integrates a general-purpose digital-signal processor, a CD-quality stereo DAC, a programmable PLL clock multiplier, a digital audio transmitter that's SPDIF (Sony/Philips Digital Interface Format) compatible, an audio serial-input port, and a serial control port. Typically, this output is connected to the input of an RS-422 optical transmitter.

The chip's programmability gives a great deal of flexibility to system architects who could easily decide to make their application software programmable. By using a control channel, a cable-TV or direct-broadcast-satellite (DBS) system could literally change the audio decode program in one million at-home boxes in a matter of seconds.

The wisdom of Crystal's decision to implement a programmable solution with a high degree of integration on-chip was proven valid in late August of this year. That's when General Instrument Corp.'s Jerrold Communications Div., Horsham, Pa., unexpectedly announced that it will use Dolby Laboratories' AC-3 audio decode algorithm in over two million cable-TV boxes. The announcement was a surprise because audio decoding using the MPEG-2 algorithm was supposed to have the inside track at GI, as has been the case in other companies where high-end systems are being designed. But many factors influence design specifications, and GI's decision has proven once again that the future of audio decoding is unpredictable.

The AC-3 coding technique, which was first used in the 1992 movie *Batman Returns*, is powerful enough to be used for home-theater and surround-sound applications, says Craig Phillips, Crystal's audio application engineer responsible for the chip. As such, it requires five DAC channels instead of the two specified in MPEG-1 and its competitor, Dolby's AC-2. Besides their additional channels, AC-3 and MPEG-2 also require more processing power of the DSP than AC-2 and MPEG-1.

Crystal's CS4920 is targeted at AC-2 and MPEG-1. It integrates just two DAC channels and can handle stereo applications, which are still expected to have a strong market presence. Dave Knapp, the CS4920's designer, says it's possible to use three chips to implement a five-channel sound system, and that as far as he knows there are no commercially available chips with five integrated DACs. Brad Fluke, Crystal's marketing manager for audio and multimedia products adds that "if AC-3 becomes dominant, we would optimize our part to do it."

Knapp goes on to say, "Crystal's design strategy has put it in a good position to rev the chip up to whatever the system designers require. A modular architecture was implemented with the modules hanging off a standard bus so that Crystal can duplicate or triplicate the DACs for as many channels as are required," says Knapp.

## DUAL-BUS DSP CORE

A wide range of signal-processing applications can be supported by the CS4920, which can deliver 16.5 million instructions/s when running on a 33-MHz clock. It features a time-multiplexed, dual-bus architecture. Its 24-bit fixed data path provides sufficient resolution for stereo and CD-quality audio applications. The execution unit has a 48-bit accumulator and no input data registers.

Much of the area in the chip's DSP block is allocated to memory. An internal 4-kword-by-24-bit SRAM is used to hold program memory, which is loaded from external ROM and contains data such as filter coefficients in addition to the program itself. An extra 2 kwords by 24 bits are reserved exclusively for such data as audio data and intermediate processing results.

Crystal's software engineers in-

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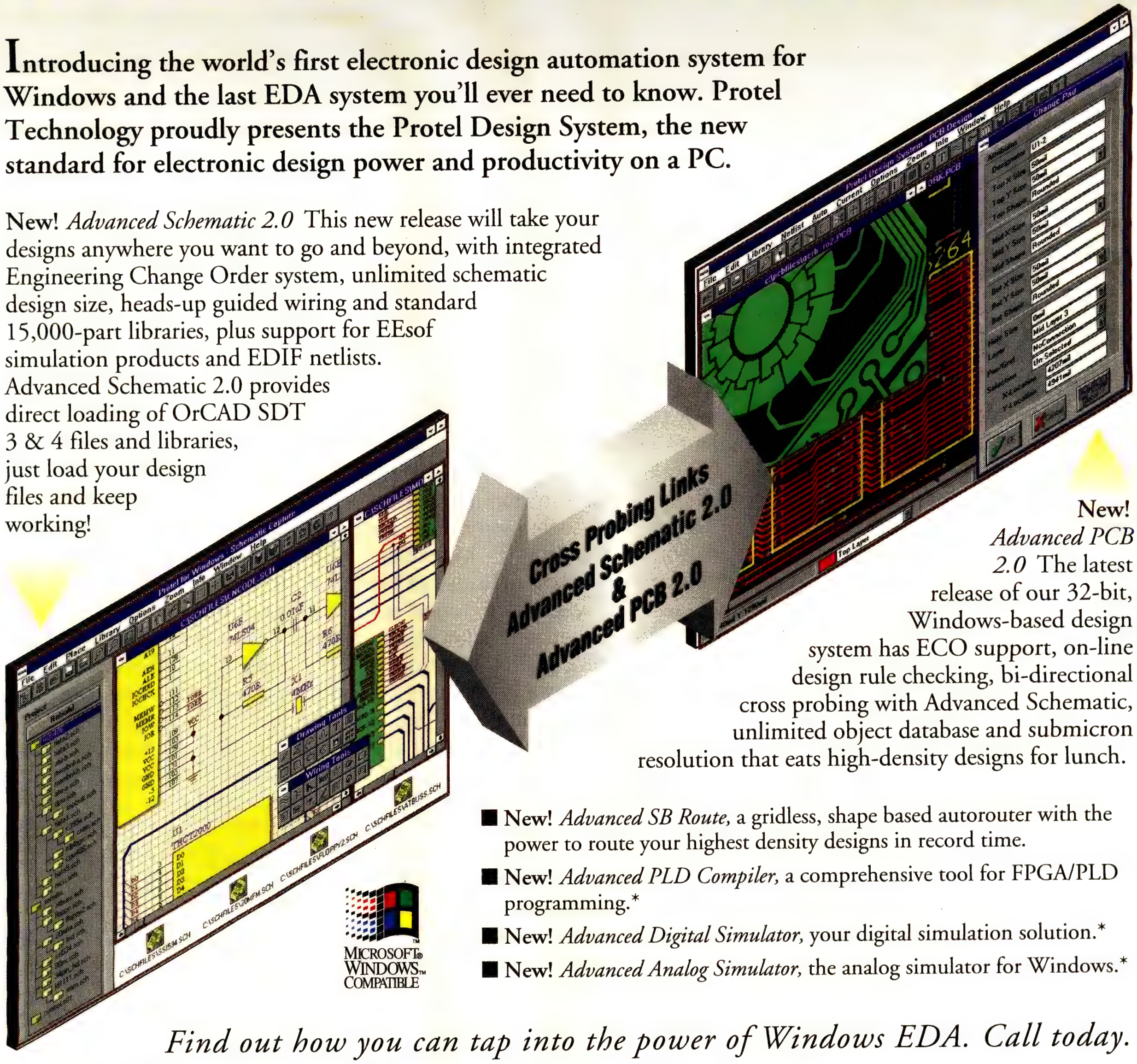

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CIRCLE 137 FOR U.S. RESPONSE CIRCLE 138 FOR RESPONSE OUTSIDE THE U.S.

tentionally created the code for the MPEG and AC-2 audio decode algorithms, available with the chip, to minimize the data space required for execution—even to the point of running extra cycles to reduce memory requirements. The chip has no input data registers. Data transfers are made from one memory location to another as a means of making writing programs for the chip easier.

Instructions take two clock cycles to complete. During the first cycle, one operand is typically read from program memory and a second operand is read from data memory. The second cycle stores the result in data memory and the next instruction is prefetched from program memory. If the system designer wishes to store the results in program memory, instead of data memory, an additional cycle is required.

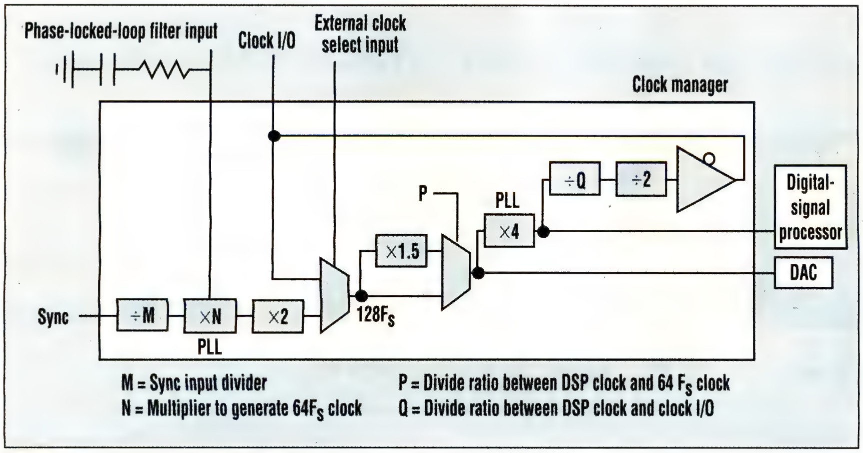
The chip's two-bus architecture consists of a destination bus and an instruction bus *(Fig. 1)*. The destination bus is connected to the data memory, the data-address unit, the input of the accumulator, one of the two inputs to the execution unit, and the I/O data bus. The instruction bus, on the other hand, connects program memory, the program address unit, the accumulator, and another input to the execution unit.

When the operands from the destination bus and the instruction bus arrive at the execution unit, the unit performs the operation specified in the instruction opcode. It can perform basic logical and arithmetic operations such as an AND, OR, XOR, ADD, and SUBTRACT. It can also multiply, multiply-and-accumulate, subtract when accumulating, and perform a divide iteration. A 48-bit accumulator register is used because the instructions require double precision.

The DSP core is designed to execute audio decompression efficiently. Although not lossless, the compression that occurs during the coding of the input signal—and the decompression that becomes the CS4920's analog output—uses a psycho-acoustical model that makes the lost data imperceptible to the ear of all but the most knowledgeable audiophiles. Conceptually, the MPEG algorithm, for example, begins by dividing the 20-kHz source audio signal into 32 subbands.

One compression technique that's used by all of the dominant algorithms in this technology arena is based on the fact that the human ear isn't nearly as sensitive to higher frequencies. So when two tones are close to each other in frequency, the higher-frequency, low-amplitude signal is masked by a lower-frequency, high-amplitude tone. This makes it possible to delete the higher-frequency, low-amplitude component of the source signal, and by doing so, compress the data stream. Additional compression is achieved by matching the bit-resolution of the signal component to the sensitivity of the human ear.

For instance, the ear hears 3-kHz frequencies very well, so the 3-kHz component of the data stream is coded at 16-bit resolution. On the other hand, most people can't hear sound at 15 kHz and above, so only a few bits are used to code the components in the 15- to 20-kHz band.


Phase-locked-loop filter input
Clock I/O
External clock select input
Clock manager
P
PLL
÷Q
÷2
Digital-signal processor
×1.5
×4
DAC
Sync
÷M
×N
×2
128F$_S$
PLL
M = Sync input divider
N = Multiplier to generate 64F$_S$ clock
P = Divide ratio between DSP clock and 64 F$_S$ clock
Q = Divide ratio between DSP clock and clock I/O

**2. A PROGRAMMABLE CLOCK MANAGER takes any sync input from 7 kHz to 40 MHz and produces all of the internal clocks required to run the DSP core and the audio peripherals. Two phase-locked loops are involved: the first generates a clock that's 128 times the audio-sampling rate; the second PLL generates the DSP clock.**

Subband coding is used to process the 32 frequency divisions that the MPEG algorithm imposes on the audio source. Within each of the 32 subbands, the signal is divided into digital frames a few milliseconds in length. Once in each frame, the maximum level attained by each subband signal is quantized and transmitted. Each subband is quantized with a bit allocation that is based on the so-called masking thresholds of the psychoacoustical model just described. Subband coding is employed instead of transform coding, in which the samples are converted from the frequency to the time domain. This is because by avoiding the time-frequency-time conversion, subband coding reduces the degree of signal processing complexity. it also avoids problems with time-domain windowing and optimizes the distribution of quantizing noise and the bit error rate across the spectrum.

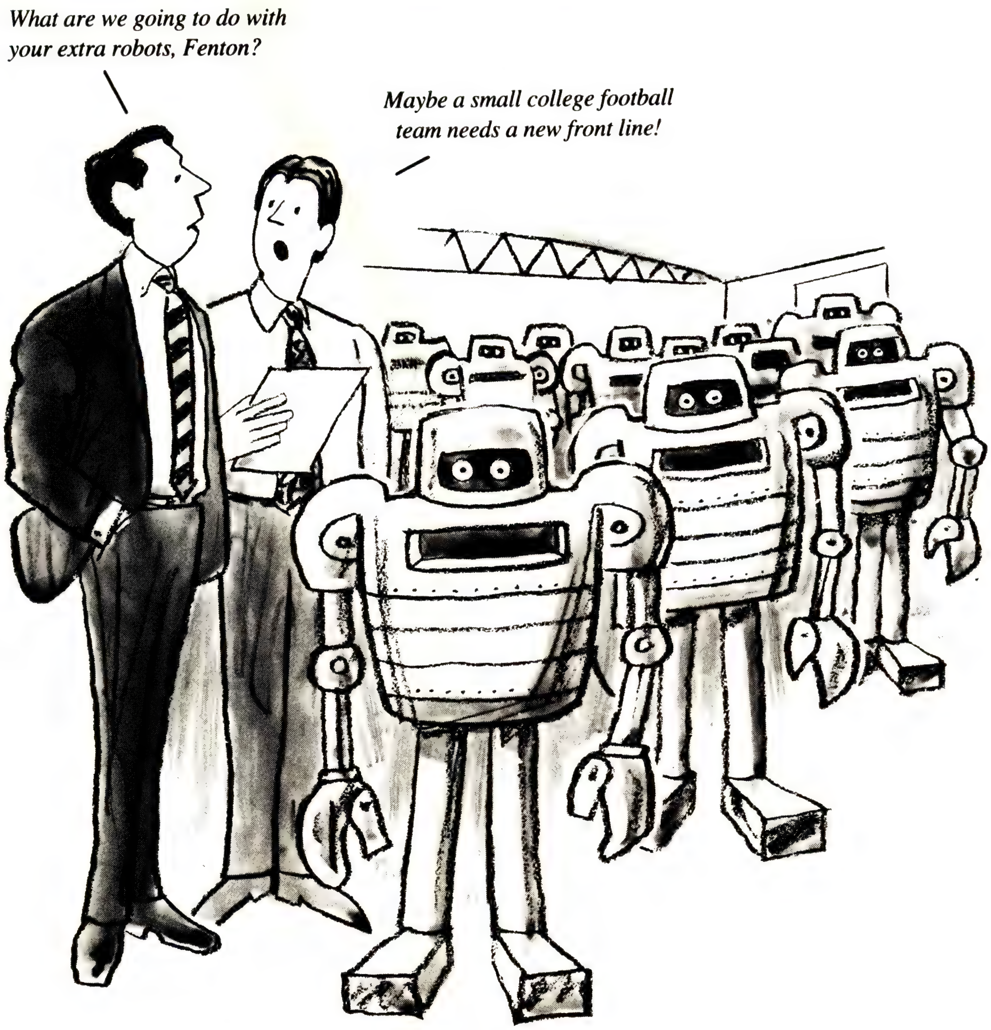
Audio decompression using the MPEG algorithm simply involves implementing the inverse filter bank that was used for compression, which is what decode chips like the CS4920 accomplish.

## PERIPHRAL CIRCUIT BLOCKS

On the output side of the chip, the stereo DACs provide a signal-to-noise ratio of 90 dB and use the sigma-delta architecture that Crystal pioneered in the late 1980s. Most of the reconstruction process is executed by the DAC's switched-capacitor filters, but an external, single-pole, passive filter is needed to complete the reconstruction of the original analog audio data.

Because synchronization is so critical in audio applications, system designers will find that one of the most valuable on-chip blocks is the clock manager *(Fig. 2)*. It uses a programmable PLL to generate all of the internal timing operations and all of the clocks needed by the DSP and audio peripherals from a sync input frequency of 7 kHz to 40 MHz.

CIRCLE 176 FOR U.S. RESPONSE →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The first of two PLL circuits on the CS4920 generates clocks at a frequency of either 128 times or 192 times the audio sample rate (i.e., $128F_s$ or $192F_s$). This is used as the DAC oversampling clock. The frequency range of this PLL is 3.2 to 7.1 MHz, which corresponds to audio sample rates of approximately 25 to 55 kHz. If the sync input has a frequency equal to the compressed data rate, all combinations of bit rates and sample rates specified in the MPEG algorithm are possible, including a sync equal to 27 MHz with audio sample rates equal to 32 kHz (the sample rate chosen for digital radio broadcast), 44.1 kHz (CD audio's sample rate), and 48 kHz (digital audio tape or DAT's sample rate). The ability to handle a 27-MHz sync is valuable in MPEG applications that have a combined audio and video bit stream because a 27-MHz clock is used to separate the MPEG bit stream's audio and video components.

Ater the first PLL generates the $128F_s$ or $192F_s$ clock, the system designer can opt to put either a $128F_s$ or $192F_s$ clock on the internal clock line. This clock is used by the stereo DAC and determines the oversampling ratio. The second PLL multiplies the $128F_s$ or $192F_s$ clock by four to generate the DSP clock, which can be any value between 20 and 40 MHz. Crystal has, however, rated the maximum frequency for the digital-signal processor in a commercial-temperature range at 33 MHz.

The dual-channel DAC is a delta-sigma converter that delivers a signal-to-noise ratio greater than 90 dB and has a total-harmonic-distortion specification of less than 0.01%. It features a passband of 20 Hz to $0.417F_s$ with less than $\pm 0.1$ dB of ripple. This means the passband extends from 20 Hz to 20 kHz at a 48-kHz sample rate.

Baseband audio is interpolated to $128F_s$ before going into the modulator. The modulator is third order and is followed by a 1-bit DAC/switch capacitor filter. The interpolation filter produces images which are attenuated by at least 60 dB from $.584F_s$ to $64F_s$. The out-of-band quantization noise from the delta-sigma modulator extends from $.417F_s$ to $64F_s$. The noise is attenuated by the switch-capacitor filter and continuous-time filters.

For applications that require a digital audio output, such as MiniDisc or Compact Digital Cassette players, Crystal implemented a transmitter on-chip that's compatible with both the SPDIF and AES/EBU (Audio Engineering Society/European Broadcasting Union) standards.

Crystal also built versatility into the CS4920's serial control port, which is compatible with either the I$^2$C or SPI standard operating modes. It performs 8-bit transfers in both modes and is always configured as a slave so it can't drive the clock signal nor initiate data transfers. The port, which is an asynchronous interface, provides interrupts and handshaking signals to ease communication between the DSP and an off-chip microcontroller.

## DEVELOPMENT TOOLS

Crystal will supply audio-decode software for MPEG Layers 1 and 2 and for Dolby Laboratories Inc.'s AC-2 algorithm. For those brave souls who prefer to write their own software, or have an application in mind for the chip other than standards-based audio decoding, Crystal provides an extensive suite of applications-development tools, including an assembler, simulator, and debugger. The tools run on an IBM-compatible PC. The PC can load programs on the chip, set breakpoints, read and write registers and memory, and execute single-step programs. To make life a little easier for system designers, the simulator and the debugger have the same menu-driven graphical-user interface. The bit includes an evaluation board and two cables that connect the PC's parallel port to the chip's debug and serial-control ports.

The straightforward on-chip debug circuitry includes a serial debug port and debug ROM. The debug ROM contains the interrupt-service routine that interprets commands sent from the PC. When the PC sends a command to the debug port, the main program or the boot program that's running at the time is interrupted and program control is switched to the debug program. After the appropriate debug commands and procedures are executed, the debug program issues a return-from-interrupt (RTI) command and program control switches back to the main program.

Breakpoints are set by replacing the instruction at the desired breakpoint location with a Trap instruction. Once the breakpoint is set and the processor's registers are initialized, the system designer issues a command that runs the main program until the Trap instruction is executed. At that time, the debug program takes over program control. The debug port and the Trap instruction can interrupt the processor independent of the interrupt-enable bit's state. This debug interrupt can be enabled or disabled by setting or clearing the debug interrupt-enable bit. The bit's default state, which is enabled, becomes cleared when a debug interrupt occurs. It gets set when an RTI instruction is executed. The high 32 words of data memory are used by the debug program.

Although Crystal expects that most of CS4920's applications will address audio decoding—especially in broadcast receivers, cable boxes, and CD-ROM players that can handle compressed audio—the chip can be programmed to perform virtually any filtering function. It could, for example, help generate sounds and create an analog output. Another likely application, enabled by the fact that it has two DACs, would be to implement a digital crossover for speakers. In this case, digital audio data would be split into two parts and routed to the tweeter and woofer.☐

## PRICE AND AVAILABILITY

*The CS4920 is fabricated in a 0.8-µm single digital CMOS process and is packaged in a 44-pin PLCC. It operates on a 5-V supply and has an operating-temperature range of 0 to 70°C. Available now, the CS4920 is priced at $38 in 1000-unit purchases. The software-development-tools package and evaluation board is priced at $500.*

*Crystal Semiconductor Corp., P.O. Box 17847, 4210 S. Industrial Dr., Austin TX; Daryl Sartain, (512) 442-7555, ext. 572; fax: (512) 462-2723.* **CIRCLE 513**

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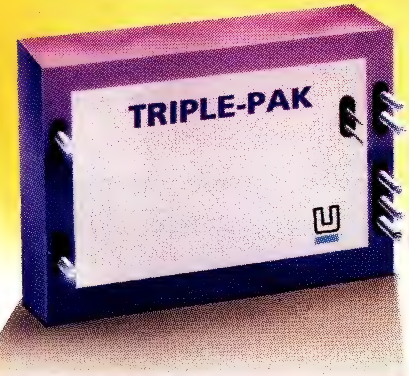

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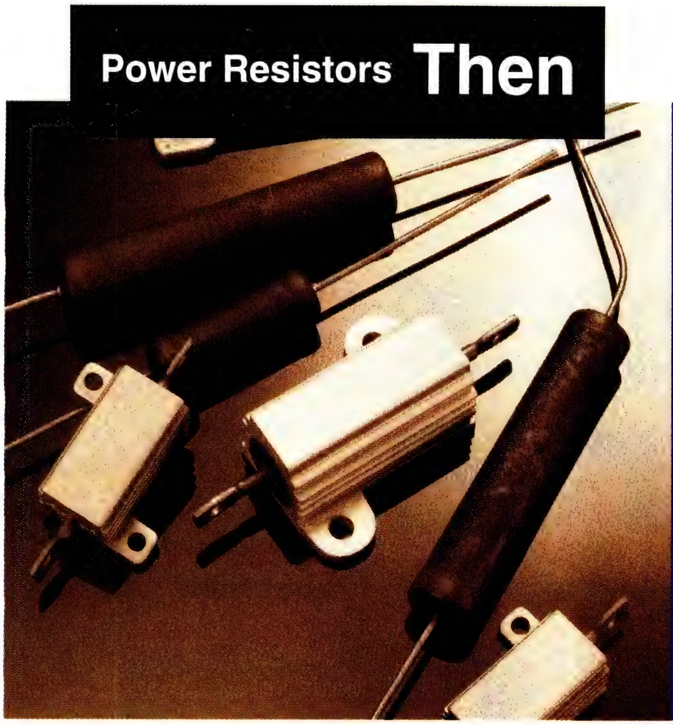

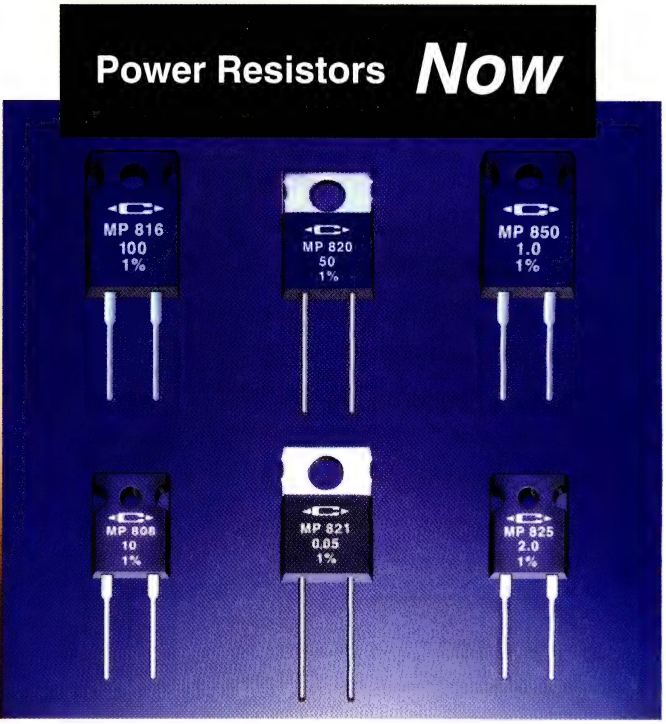

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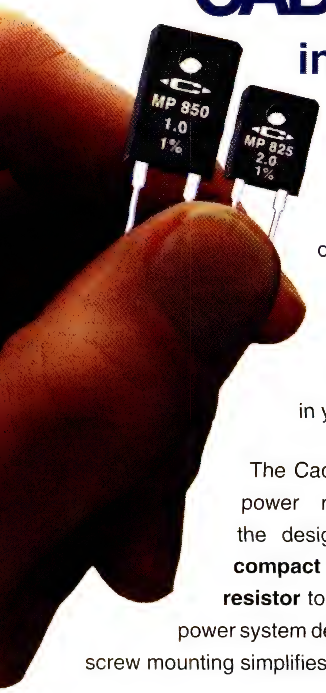

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| TO-220 Style Package | **MP 816** | 16 Watts | 0.10 Ω to 10K | Thermally Conductive Molded Package |
| | **MP 850** | 50 Watts | 1.0 Ω to 10K | Copper Heat Sink Integral in the Molded Package |
| TO-220 with Metal Mounting Tab | **MP 820** | 20 Watts | 10.0 Ω to 10K | Metal Mounting Tab |
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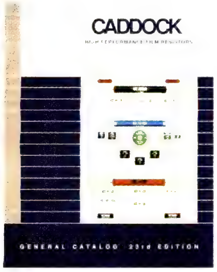

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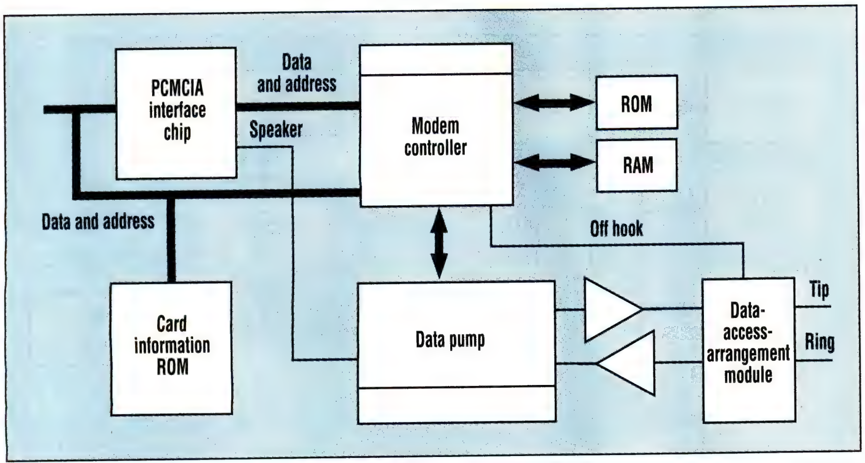
CIRCLE 152 FOR U.S. RESPONSE

CIRCLE 153 FOR RESPONSE OUTSIDE THE U.S.



COURTESY: SMART MODULAR TECHNOLOGIES

# SOPHISTICATION SPURS ON MODEM TECHNOLOGY

**MILT LEONARD**

## DSP-BASED MODEM CHIPS BRING MORE SPEED AND FUNCTIONALITY TO TRADITIONAL AND NEW APPLICATIONS.

Despite its maturity, modem technology is characterized by remarkably dynamic change. Driven by digital-signal-processing (DSP) techniques, modem chip sets with increased transmission speeds and expanded feature sets are bringing sophisticated data, fax, and voice communications capabilities to an expanding range of applications.

At the high end, modem speeds are exceeding the limits of analog transmission lines and entering the digital realm of high-speed communications networks. At the other end, low-cost multifunctional modem chips are bringing data, fax, and voice services into the home. In between these two extremes, various chip- and board-level products provide the means for creating unique modem solutions for any application.

Functionally, a modem consists of five major blocks. These include a data-access arrangement (DAA) that interfaces to the telephone line, an analog front end with optional I/O for speakers and microphones, a DSP circuit that executes modulation algorithms stored in local memory, a microcontroller that performs data compression and error correction, and an interface to the host system *(Fig. 1)*.

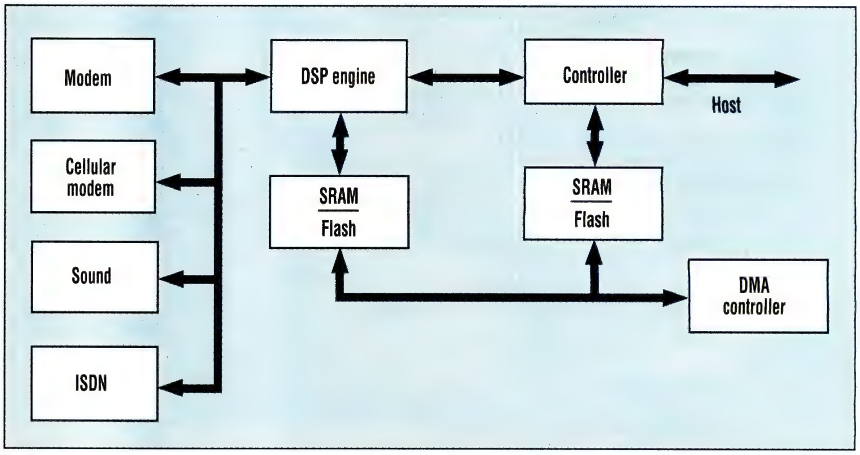
This basic architecture has remained relatively unchanged over the years. Despite this fact, improved circuit design and signal-processing techniques have escalated data rates to the point of approaching the theoretical limits of telephone transmission lines.

For voice-grade telephone lines, this limit is traditionally held to 20 kbits/s at an available bandwidth of 3 kHz. However, modem makers are stretching beyond this limit by using sophisticated DSP techniques, such as line probing, multidimensional trellis coding, signal shaping, and protocol spoofing. The combined result is more efficient use of available bandwidth.

Line probing involves two linked terminals that exchange a predetermined signal sequence in a handshaking operation to determine the optimum baud rate, carrier frequency, and coding technique for existing line conditions. Multidimensional trellis coding is a forward-error-correcting scheme that improves signal-to-noise performance. In signal shaping, frequently occurring signal points are transmitted at higher power, and less frequent points at reduced power. The net effect is improved average signal-to-noise performance. Protocol spoofing strips redundant protocol overhead for faster data transfers.

These speed-enhancing techniques are among the chief ingredients of the proposed V.fast standard, which supports uncompressed data rates from 19.2 to 28.8 kbits/s *(see "V.fast: The ultimate modem?," this page)*. Although the standard is nearing completion by the CCITT (Consultative Committee for International Telegraphy and Telephony), a consortium of 18 communications companies announced early this year its support of V.32terbo, a de facto standard that implements a similar modulation scheme at a rate of 19.2 kbits/s.

V.32terbo, which is an extension of the 14.4-kbit/s V.32bis standard, has been implemented in a data-pump chip set from AT&T Microelectronics, Berkeley Heights, N.J. Developed by AT&T for its video phone and introduced to the OEM market early this year, the data-fax chip set consists of a codec, a data-pump interface, and a DSP chip coded for V.32terbo modulation.



**1. A BASIC MODEM ARCHITECTURE,** which has remained virtually unchanged over time, consists of a simple arrangement of an analog front end, a DSP section, and a microcontroller with associated local memory. However, with the addition of cellular, sound, ISDN, flash memory, and DMA control, future designs will be enhanced for even greater functionality.

To be compatible with V.32 modems, key features in V.32bis modems are unchanged in the V.32terbo standard. V.32terbo modems connect to other V.32 modems at the highest rate supported by both types. The V.32terbo standard also covers such modem features as fast-rate change, initial-rate negotiation, autorating, and automoding. By using compression schemes such as those specified in the NMP5 and V.42bis standards, the data rate for V.32terbo modems can increase up to 115.2 kbits/s.

This past July, Rockwell International, Newport Beach, Calif., announced its V.FC (V.Fast Class) family of data/fax modems with similar transmission capabilities. The product family includes both data pumps and integrated-mode solutions. The data pump connects to the host

## V.FAST: THE ULTIMATE MODEM?

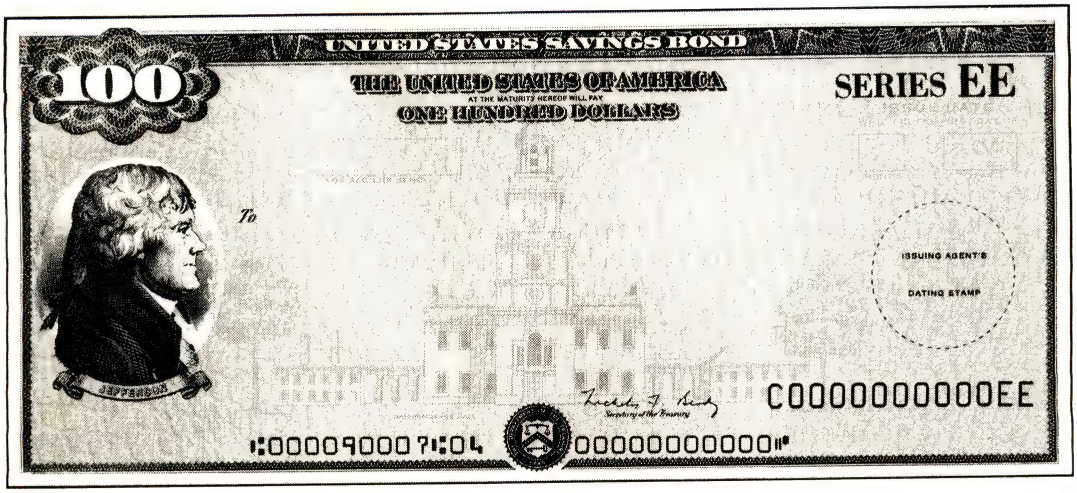
The term "V.fast" is the working name for a forthcoming international standard that will support data rates up to 28.8 kbits/s over ordinary dial-up telephone lines. Currently, the highest standardized data rate is 14.4 kbits/s as specified in the V.32bis standard. At 14.4 kbits/s, V.fast will double this rate and nearly approach the theoretical telephone-line capacity.

Unlike V.32 modems that operate at a fixed bandwidth of 2400 Hz, V.fast modems will be able to use bandwidths of up to 3.429 kHz, depending on channel characteristics. Sophisticated line-probing techniques will be used to measure line characteristics, followed by advanced equalization techniques (such as precoding and adaptive preemphasis) to exploit the maximum possible bandwidth. V.fast modems will also employ multidimensional trellis coding and shaping, adaptive power control, and other advanced technologies to maximize line use. There will be backward compatibility with V.32bis, V.32, and earlier dial-up modems.

This past July, the V.fast Rapporteur Group of the International Telecommunications Union (ITU) Telecommunications Standards Sector (formerly CCITT) agreed on all major features of the V.fast standard. Drafting of the standard is now underway. Many details still need to be resolved, the most complicated of which is specification of the startup procedure. The Rapporteur group expects to arrive at a firm draft by this December. Meeting this deadline would allow several months of testing to verify performance and interoperability before submitting the final V.fast text for balloting in March 1994.

Because all major modem manufacturers have been closely involved in the standard's development, V.fast modems should be available soon after the standard is finalized. Because V.fast technology is currently being engineered into VLSI chips, pricing is expected to follow the pattern set by V.32 and V.32bis modems.

*Written by David McNamara, director of product planning for Transmission Products, Motorola Codex.*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through a V.24 serial interface and microcontrollers.

Operating over the public switched telephone network, a V.FC modem complies with V.32bis, V.32, V.22bis, V.22, V.29, V.27ter, V.26bis, V.26A, V.23, and V.21 international standards, and supports the Bell 212 and 103 specifications in the U. S. Fax functions support Group III send/receive transmission speeds from 14.4 kbits/s down to 2.4 kbits/s and meet CCITT V.17 recommendations. Like AT&T's V.32terbo, the V.FC standard will be upgradable to the V.fast standard when it's eventually finalized.

Because V.fast is on the threshold of becoming an international standard, the modem community is split between going with V.terbo now or waiting for V.fast standardization. Aggressive external modem vendors in both camps are already announcing products. Among the early implementations of V.terbo technology is the Z32b-SZ external modem family from Zypcom Inc., Hayward, Calif., which uses the AT&T chip set. Operating in DOS, Windows, Mac, and AS/400 environments, the full-duplex data/fax modems run over dial-up and leased telephone lines with automatic dial backup and restore features.

Prior to the availability of Rockwell's V.FC chips, Motorola Codex, Mansfield, Mass., developed an external modem based on the proposed V.fast technology. The core technology of the 326XFast-SDC modem is a set of algorithms executed by general-purpose DSP software, providing a full-duplex throughput of 72 kbits/s, synchronously, and 115.2 kbits/s, asynchronously, over standard voice-grade analog lines. The modem uses a modified V.42 error-correction protocol and a modified V.42bis data-compression algorithm with compression ratios up to 4:1.

The modem provides a more economical alternative to switched 56 (SW56) or ISDN services in a networked environment by combining V.fast technology with synchronous data compression (SDC). This technique preserves HDLC/SDLC frame integrity for transmission across an analog link without any jitter or delay.

Analog modems, possessing speeds below the V.fast specification, operate over voice-grade telephone lines for data, fax, and voice applications. Next-generation higher-speed modems will enter the digital domain for Group IV fax, wide-area network, and video applications. Yet, with an estimated 160 million miles of copper cable in place and new copper still being installed, telephone companies are expected to rely on existing copper lines well into the next century. This means copper performance must be upgraded until optical fiber becomes entrenched.

According to Level One Communications Inc., Folsom, Calif., HDSL (high-bit-rate digital subscriber line) technology can be used to bridge the gap between today's technology and tomorrow's needs. HDSL technology will allow telephone companies to use existing copper-cable plants while meeting demands for updated services, including faster modem transmissions.

Developed for twisted-pair transport, HDSL technology is an enhanced version of the T1/E1 transmission system devised by Bell Telephone for digital voice and data communications. Traditional T1 or E1 takes digital data directly from a source, such as a computer modem, or digitizes analog signals from a subscriber's telephone. These signals are transmitted in digital form to the receiving end of the link where digitized voice signals are reconverted to analog form. Because digital signals can be multiplexed, T1/E1 extends the capacity of existing copper cabling by enabling each cable to carry more traffic.

HDSL technology uses adaptive echo cancellation and equalization, analog-to-digital and digital-to-analog conversion, advanced filtering techniques, and 2B1Q line coding. These complex signal-conditioning operations and long transmission distances require VLSI implementations with mixed-signal circuits to get DSP power exceeding 300 MIPS.

T1 carrier signals transmit information at 1.544 Mbits/s over two pairs of copper wire (one way on each pair) and can transmit simultaneously on 24 channels. HDSL's dual-duplex (two-way) 784-kbit/s transmission rate allows it to carry the same data payload on two pairs of wires over 36 channels of 64 kbits/s each. Where T1 requires a repeater every 3000 to 5000 feet, HDSL has a 10,000-ft. range without the need for using repeaters.

In addition, HDSL eliminates much of the cable conditioning that

**2. THIS MODEM BOARD** allows modem suppliers to configure a variety of personal communications products from a single DSP-based architecture. The board employs the 14.4-kbit/s SQ3220 IC designed by Sierra Semiconductor and combines fax, voice-mail, caller-ID, and sound-playback features.

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Your customers and prospects agree that trade shows are worth attending. But they also agree that specialized business publications are worth a great deal more to them. Because that's where they find more of the important information they need to know. A recent study, conducted by the Forsyth Group, proves it.

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T1 installations require, such as the use of a single wire size and costly grooming to accommodate bridge taps. In contrast, HDSL functions, which feature a variety of cable gauges, support bridge taps and can usually be installed by changing interface cards at each end of a link.

HDSL functions are performed by HDSL transmission units installed at either end of the T1/E1 link. Both units contain a data-pump circuit for each wire pair that extracts data and timing information from the incoming signal and produces a stream of binary data. This data passes to a framer/multiplexer chip that interlinks data from the two data pumps, inserts the T1/E1 framing bit which identifies each signal, and sends the signal to a T1/E1 interface chip. At the subscriber end, the interface chip sends long-haul signals to the customer interface. At the central office, the interface chip serves the needs of short-haul transmissions inside the central office.

This past April, Level One introduced the first single-chip implementation of the HDSL interface. The chip performs all of the functions offered by existing board-level HDSL data pumps, including high-resolution data conversion, transmit-receive filters, timing circuitry, line drivers, and multiple DSP engines. Widespread deployment of HDSL systems is expected to begin by mid-1994. Predictions are for 100,000 HDSL lines in North America by the end of next year.

## MORE FUNCTIONALITY

Not all modem-chip makers have joined the race for higher data rates. "Modem speed is becoming secondary to multifunctionality," says Dr. Hamdi El-Sissi, president and CEO of Phylon Inc., Fremont, Calif. Dr. El-Sissi also said that over the past five years, modem technology has been in transition from being hardware-intensive to becoming software-intensive. "Our software design effort is now three times that for hardware," he adds.

Increasing modem functionality by encapsulating software in silicon is the approach Phylon uses for its PHY1003 modem chip set. The set integrates V.42bis compression with V.32bis operation for data, fax, and voice applications with 115.2-kbit/s or 57.6-kbit/s performance. The PHY1003 consists of two CMOS VLSI chips: a DSP engine that executes the company's modem software, and a mixed-signal analog front end. The chip set is used with inexpensive 8-bit microcontrollers, such as the 8032 from Intel Corp., Santa Clara, Calif., or the Z8 from Zilog Corp., Campbell, Calif.

The PHY1003's voice-compression algorithm encodes voice at 14.4 kbits/s. Other features include data, fax, and voice detection; DTMF (dual-tone, multiple-frequency) and programmable tone-generation and detection; a caller-ID receiver; and a low-power sleep mode. Depending on the implementation, Phylon-based modems can be upgraded to comply with V.32terbo and V.fast standards by downloading new algorithms over dial-up lines, by using a floppy disk, or by changing an

### CCITT V-SERIES MODEM PERFORMANCE SUMMARY

| Mode | Max. rate (bits/s) | Modulation scheme | Symbol rate (baud) | Carrier (Hz) | Communication type | Synch./ asynch. |
|---|---|---|---|---|---|---|
| V.17 | 14,400 | QAM | 7400 | 1800 | FD | Synch. |
| V.21 | 300 | FSK | 300 | 1750/1080 | FD | Either |
| V.22 | 1200 | PSK | 600 | 2400/1200 | FD | Either |
| V.22bis | 2400 | QAM | 600 | 2400/1200 | FD | Either |
| V.23 |  | FM | 1200 | 2100/1300 | HD | Either |
| V.23 |  | FM | 75 | 450/390 | FD | Either |
| V.26 | 2400 | PSK | 1200 | 1800 | FD | Synch. |
| V.26bis | 2400 | PSK | 1200 | 1800 | HD | Synch. |
| V.26ter | 2400 | PSK | 1200 | 1800 | HD/FD | Either |
| V.26ter | 1200 | PSK | 1200 | 1800 | HD/FD | Either |
| V.27 | 4800 | PSK | 1600 | 1800 | HD/FD | Synch. |
| V.27bis | 4800 | PSK | 1600 | 1800 | HD/FD | Synch. |
| V.27bis | 2400 | PSK | 1200 | 1800 | HD/FD | Synch. |
| V.27ter | 4800 | PSK | 1600 | 1800 | HD | Synch. |
| V.27ter | 2400 | PSK | 1200 | 1800 | HD | Synch. |
| V.29 | 9600 | QAM | 2400 | 1700 | HD | Synch. |
| V.29 | 7200 | PSK | 2400 | 1700 | HD | Synch. |
| V.29 | 4800 | PSK | 2400 | 1700 | HD | Synch. |
| V.32 | 9600 | QAM | 2400 | 1800 | HD/FD | Synch. |
| V.32 | 4800 | QAM | 2400 | 1800 | FD | Synch. |
| V.32bis | 14,400 | TCM | 2400 | 1800 | FD | Synch. |
| V.32bis | 12,000 | TCM | 2400 | 1800 | FD | Synch. |
| V.32bis | 9600 | TCM | 2400 | 1800 | FD | Synch. |
| V.32bis | 7200 | TCM | 2400 | 1800 | FD | Synch. |
| V.32bis | 4800 | TCM | 2400 | 1800 | FD | Synch. |
| V.32terbo | 19,200 | TCM | 2400 | 1800 | FD | Synch. |
| V.32terbo | 16,800 | TCM | 2400 | 1800 | FD | Synch. |
| V.32terbo | 14,000 | TCM | 2400 | 1800 | FD | Synch. |
| V.33 | 14,000 | TCM | 2400 | 1800 | FD | Synch. |

FM = frequency modulation; FSK = frequency-shift keying; PSK = phase-shift keying; QAM = quadrature amplitude modulation; TCM = trellis-coded modulation; FD = full duplex; HD = half duplex.

## Introducing Motorola's New Single-Board Computer.

Meet the remarkable MVME197. It measures a mere 6x9 inches, but has the strength of several boards. In fact, the MVME197 is packed with more functionality, and more performance, than any single-slot 6U VME board ever designed.

On the other hand, we did have twice the room to work with. Because we put surface mount components on both sides of the board, front and back.

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The MVME197 is driven by single or dual 50 MHz RISC processors. These powerful MC88110 engines take advantage of both on-board cache and Symmetric Superscalar™ processing. Making no single-slot 6U VME board on the market a match for the lightning-fast MVME197.

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### Six Boards In One.

Now, when space is crucial, the MVME197 will do the job of six ordinary boards. So you can add more functions. Consume less power. And pay a whole lot less than you would for half a dozen peripheral boards. But what else would you expect from the leading supplier of VME boards?

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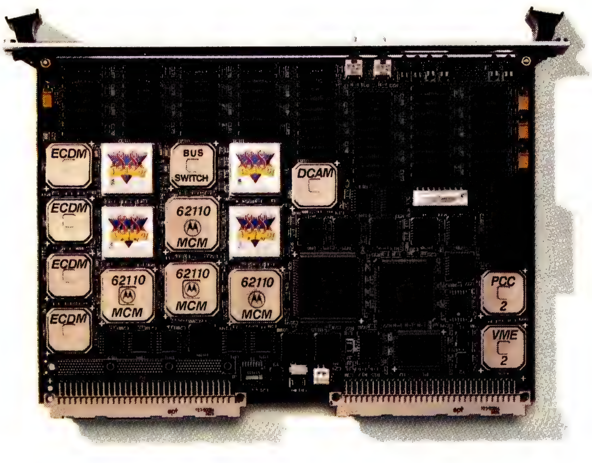
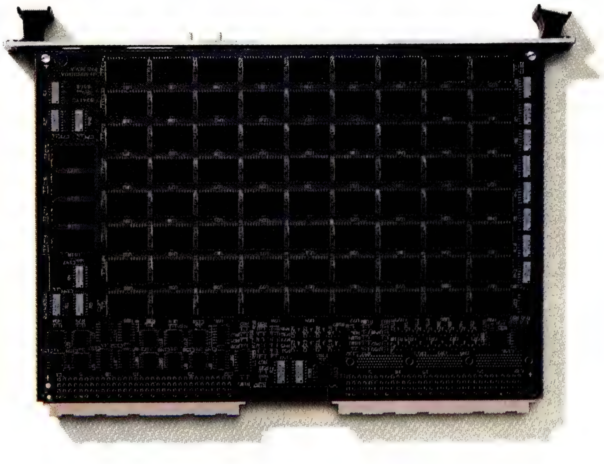


Front Side



Back Side

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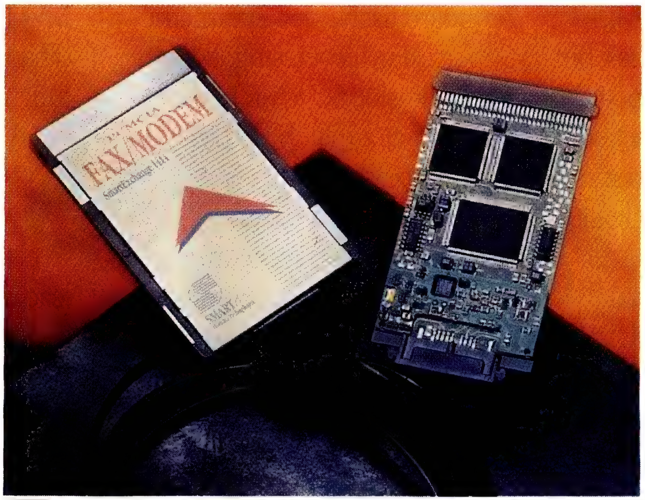
EPROM.

For flexible modem configuration, the DSP engine operates in real time from an on-board RAM. Typically, the code is stored in EPROM and then dynamically transferred to RAM for execution. Alternatively, the RAM can be loaded from flash memory to field upgrade the modem over dial-up lines, or from attached data-terminal equipment (DTE). Flash-memory size requirements can be minimized by first downloading new DSP code into system memory, and then loading the code into flash memory.



**3. PACKAGING OPTIONS** for most modem chips include thin, plastic quad flat packs for mounting inside PCMCIA cards. Removing the cover from Smart Modular Technologies' modem card reveals the three VLSI chips that implement the modem core plus support circuitry. The card easily accommodates these components with room to spare.

Caller identification is an increasingly attractive modem capability as modems move into nontraditional applications requiring computer and network security. These include biomedical diagnostics, messaging systems, automatic teller machines, security monitoring, reservation terminals, and credit-card verification. With caller ID, the receive modem can detect the phone number of the calling modem before it picks up and answers the call. This allows a networked or standalone computer to reject an unwanted call or accept calls from a number of preselected sources. The calling party can opt to suppress caller ID.

**4. A UNIQUE SOLUTION** devised by Megahertz Corp. for connecting its XJack PCMCIA-based modem to the telephone line is in keeping with the miniature scale of the card. The telephone port is an internal, extendible, stripped-down version of an RJ-11 jack. Pressing on the exposed end of the card extends the jack for connecting the port to a telephone cord.

In areas where caller ID is approved, the local telephone office generates a three-part caller-ID signal between the first and second ring. The signal consists of a series of alternating ones and zeros, followed by a marking state. The final part of the signal is the caller-ID data, which includes a date, time stamp, and checksum. The entire signal has a 450-ms duration. Upon receiving the signal, the computer can accept the call, display the calling number on a screen, and/or pass the information onto a phone-logging database.

The caller-ID signal currently is sent by about half of the local telephone offices in the U.S. and eventually will be used by every local telephone office in the U.S. and Canada. Europe and Asia are expected to adopt the caller ID feature sometime in the future.

Caller-ID capability can also be found in a family of single-chip devices from Silicon Systems, Tustin, Calif. At the top of the line, the 73K324L provides the bit rates for the V.22bis, V.22, V.21, and Bell 212A standards. The chip interfaces with popular microprocessors and uses a serial or parallel microprocessor bus for control. Included on the device are selectable synchronous or asynchronous operation with internal buffer/debuffer and scrambler/descrambler functions, and adaptive equalization.

Voice and audio capability are appearing in a growing number of so-called full-featured modem chips and chip sets. One example is Rockwell's recently introduced RC14V42AC two-chip modem that integrates fax, data, and answering-machine functions. According to product manager Mark Chapman, the 14.4-kbit/s chip set is optimized for remote PC communications, even allowing a PC to convert text to sound and have it read back over the telephone. The modem provides programmable compression rates based on sound quality and storage requirements.

Similar functionality is available in the CL-MD1414 chip sets developed by Cirrus Logic Inc., Fremont, Calif. In addition to providing up to a 14.4-kbit/s data rate in both data and fax modes, they have an integrated microphone input and a telephone-emulation feature. Telephone emulation allows users to dial from a keyboard and use a telephone headset or handset for voice communications. Complementing this feature is an embedded voice mode. With this mode, a system can function as a telephone answering machine, recording and storing messages for retrieval from a remote location. The audio interface also gives Dictaphone capability to a host PC or to a personal digital assistant.

Another example is the SQ3220 personal-communications chip set devised by Sierra Semiconductor, San Jose, Calif. This product allows modem-card designers to incorporate voice mail, caller ID, and Microsoft's Business Audio and WAV

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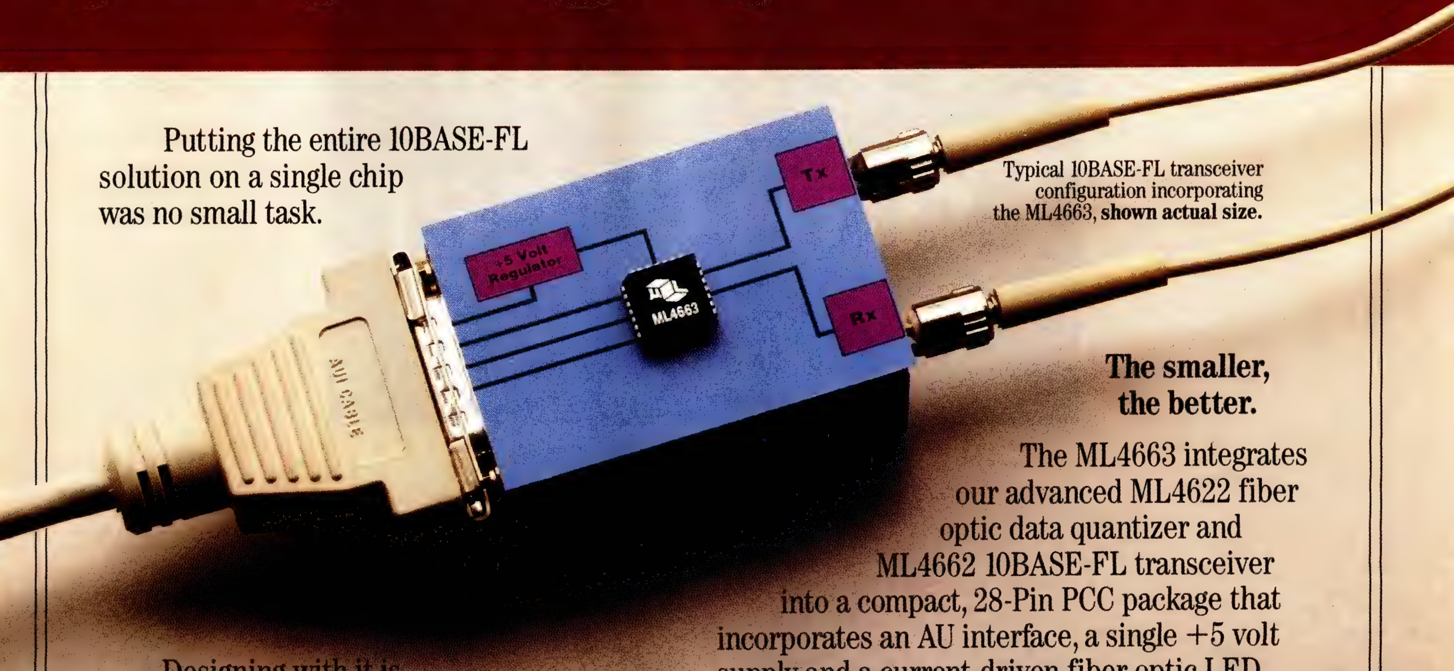

Typical 10BASE-FL transceiver configuration incorporating the ML4663, **shown actual size.**

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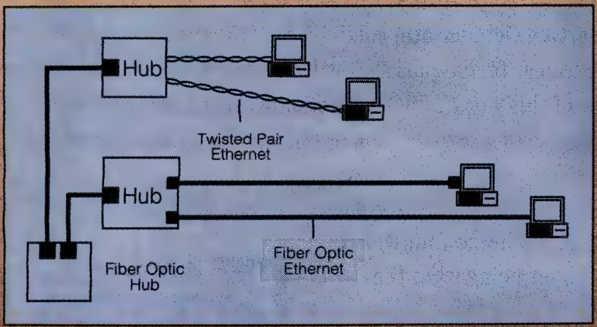

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file-sound playback features into their designs *(Fig. 2)*. The chip set has the flexibility to configure many products from the same DSP-based architecture. With 14.4-kbit/s data rates, the chip set supports Group III Class 2 faxes, as well as all popular compression and error-control algorithms.

## HOLD DOWN THE POWER

A major trend in modem design is the computer industry's push for increased miniaturization and energy conservation—particularly for portable designs. Ajay Shah, marketing vice president at Smart Modular Technologies, Fremont, Calif., remarks, "In virtually every data system equipped with a modem card—laptop, palmtop, or desktop computer—the modem continuously consumes a significant amount of power while the system operates, whether or not the modem is activated."

The company has developed a line of PCMCIA-based fax modems tailored to the needs of notebook and palmtop products *(Fig. 3)*. The SmartExchange cards offer data and fax transmission and reception at 14.4 kbits/s. With data compression and error correction, data throughput increases up to 57.6 kbits/s. A voice capability is planned for future designs.

The modems employ several schemes to save power in battery-driven computers. A standby mode automatically removes power from most of the modem's circuitry when no activity occurs for a user-programmable time period. A read, write, or ring signal returns the modem to normal operation.

In the sleep mode, a command from the host computer through the PCMCIA interface turns off the modem's power completely. Thus, the modem draws less than 2 mA of current. The modem connects to a telephone line through a cable with built-in DAA circuitry.

Supporting the trend toward lower-voltage operation, Rockwell developed the industry's first 3.3-V family of V.32/V.32bis data/fax/voice modems. These modems consume one-third the power of comparable 5-V devices. For use in portable communications, the RC144AGC consists of a data pump and microcontroller. Power consumption is 250 mW in the active mode and 15 mW in the sleep mode.

Most PCMCIA-based modems avoid the problem of plugging standard telephone connectors into a 5-mm thick card by including an adapter cable. However, Megahertz Corp., Salt Lake City, Utah, devised a connection scheme that does away with the bulk and awkwardness of cabling. The company's XJack data-fax modem, available in 2400- and 14.400-bit/s models, has a retractable stripped-dowm RJ-11 port that hooks to a phone jack through a standard telephone cord *(Fig. 4)*. Users eject the port by pressing against the exposed end of the card. Once the data transfer is completed, the cord is removed and the port is pushed back into its internal locked position.

Another factor influencing modem design—especially for fax communications—is the growing use of fax machines in the home. "We believe the sales of home fax machines will eventually overtake the sales of business fax machines, explains Judith Pirani, director of Image Communication Systems Market Advisory Service at BIS Strategic Decisions, Norwell, Mass.

This year, Intel Corp., Santa Clara, Calif., introduced a line of low-cost, internal and external fax modems so that small-office and home users can communicate with electronic services, access electronic bulletin-board systems, or communicate with an office from home. Users can also send or receive fax messages from their PCs.

This market is being supported by low-cost fax chip sets, such as the R96PFE chip set available from Rockwell, which consists of a 9600-bit/s fax-modem chip and a microcontroller. Specifically targeting the home fax-machine market, the device set integrates the modem interface with all of the necessary control functions for the printer, scanner, and keyboard.☐

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# SCTC ANALYSIS ESTIMATES LOW-FREQUENCY –3-dB POINT

## USE SHORT-CIRCUIT TIME CONSTANTS TO GUIDE THE CHOICE OF BYPASS- AND COUPLING-CAPACITOR VALUES IN LINEAR-CIRCUIT DESIGN.

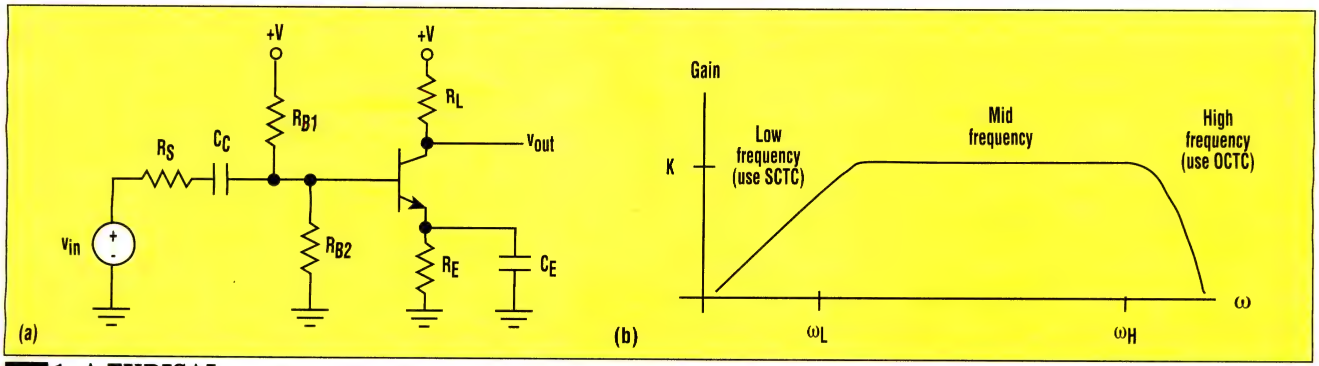
**MARC THOMPSON**
Polaroid Corp., 153 Needham St.,
Bldg. 1, Newton, MA 02164;
(617) 386-4465.

Open-circuit time constants is a method for approximating the high-frequency –3-dB point ($\omega_H$) that was detailed in a previous article (ELECTRONIC DESIGN SPECIAL ANALOG ISSUE, *June 24, 1993, p. 41)*. An analogous short-circuit time constants (SCTC) procedure allows designers to approximately calculate the low frequency –3-dB point ($\omega_L$) of a linear circuit using the circuit's low-frequency incremental model.

The complete model for a typical ac-coupled transistor amplifier has four capacitors in it, two of which are due to internal transistor capacitances *(Fig. 1a)*. In many instances, the transistor amplifier has a wide mid-frequency range where gain is constant *(Fig. 1b)*. Therefore, the amplifier's full incremental model can be split into three simpler models—low frequency, mid-band, and high frequency.

In the low-frequency amplifier model, the effects of bypass and coupling capacitors dominate, and internal transistor capacitances behave as open-circuits. The mid-band model can ignore the effects of all circuit capacitances. In the high-frequency amplifier model, internal transistor capacitances dominate, and all bypass and coupling capacitors behave as short-circuits.

It's simple to determine the form of the transfer function for the amplifier



**1. A TYPICAL** ac-coupled transistor amplifier (a) has a wide mid-frequency range in which gain is constant (b). Consequently, the full incremental model can be split into three simpler models.

in Figure 1a if only low- and mid-frequency behavior is considered. In addition, the analysis won't account for high-frequency behavior due to internal transistor capacitances. The circuit has two capacitors, so there are two independent poles in the transfer function. Also, there's a zero at zero frequency due to the coupling capacitor $C_C$. Finally, there's a zero at higher frequency due to the emitter bypass capacitor $C_E$. A transfer function that meets these requirements is:

$$\frac{v_{out}}{v_{in}} = \frac{Ks(\tau_z s+1)}{(\tau_1 s+1)(\tau_2 s+1)} \qquad (1)$$

This transfer function results in the gain-versus-frequency plot that's shown in Figure 1b for low and mid frequencies. Although it won't be proven here, all zeros of the transfer function are at lower frequencies than the highest pole. Therefore, the transfer function may be approximated by assuming that the zeros are at zero frequency:

$$\frac{v_{out}}{v_{in}} \approx \frac{Ks^2}{(\tau_1 s+1)(\tau_2 s+1)} \qquad (2)$$

Multiplying out the denominator results in:

$$\frac{v_{out}}{v_{in}} \approx \frac{Ks^2}{\tau_1\tau_2 s^2+(\tau_1+\tau_2)s+1} \qquad (3)$$

Generally, each coupling and bypass capacitor has a relatively large value. This results in each time constant $\tau$ being relatively big. Therefore, throw out the +1 term in the denominator of the equation to make the following approximation valid at low frequencies:

$$\frac{v_{out}}{v_{in}} \approx \frac{Ks}{\tau_1\tau_2 s+(\tau_1+\tau_2)} \qquad (4)$$

Using standard Bode-plot methods, it is clear that the –3-dB point of this transfer function occurs when:

$$\omega_L \approx \frac{\tau_1+\tau_2}{\tau_1\tau_2} \approx \frac{1}{\tau_1}+\frac{1}{\tau_2} \qquad (5)$$

Equation 5 approximates the low-frequency breakpoint as the summation of two easily calculated frequencies. Following a line of reasoning similar to that used in open-circuit time constants analysis, the low-frequency breakpoint of a network is approximated by:

$$\omega_L \approx \sum_j \frac{1}{\tau_j} \qquad (6)$$

where each $\tau_j$ is an RC time constant of every individual bypass or coupling capacitor with all other bypass and decoupling capacitors in the circuit shorted. Even though this example works through the math for a circuit with two capacitors, the method may be with equal validity to networks with more bypass and coupling capacitors.

## DESIGN EXAMPLE

Consider the design of a single-transistor amplifier *(Fig. 2)*. The circuit uses a 2N3904 transistor, and has the following design specifications: a source resistance $R_S$ of 1 kΩ, gain of greater than 100, and a low-frequency –3-dB point $f_L$ of less than 1 kHz.

The SCTC analysis considers only the low-frequency behavior of the amplifier. Bias-point and load-resistor values have been chosen to give a mid-band gain of approximately –100. SCTC will help select reasonable values for the capacitors $C_C$ and $C_E$ based on the specification of low-frequency –3-dB point.

The transistor has the following parameters: collector current, $I_C$ is 2 mA; $r_x$ is 160 Ω; $r_\pi$ is 2.6 kΩ; $g_m$ is 0.08 mho; and $h_{fe}$ is 200 *(Fig. 3a)*. The two short-circuit time constants for $C_C$ and $C_E$ are to be called $\tau_1$ and $\tau_2$. SCTC show that to meet the bandwidth specification, the following must hold:

$$\frac{1}{\tau_1}+\frac{1}{\tau_2} < 2\pi \times 1000 \qquad (7)$$

To find $\tau_1$, the short-circuit time constant for $C_C$, first turn off the input source $v_{in}$ by shorting it. Then, short circuit $C_E$ and find the resistance $R_{1s}$ across the $C_C$ terminals *(Fig. 3b)*. The time constant $\tau_1 = R_{1s}C_C$. Because a brief inspection reveals that the $g_m v_\pi$ generator has no effect on $R_{1s}$, the resistance is:

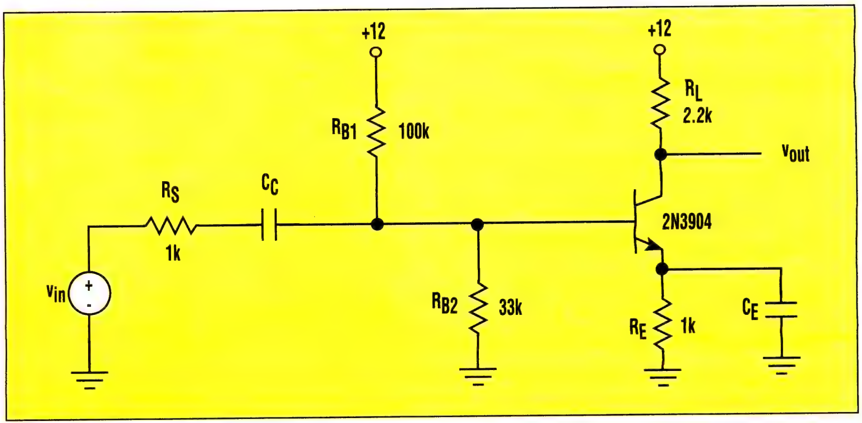
$$R_{1s} = R_s + (R_{B1} \| R_{B2}) \| (r_x + r_\pi) \approx 3.5\ \text{k}\Omega \qquad (8)$$

Find $\tau_2$, the short-circuit time constant for $C_E$, by short circuiting $C_C$ and calculating the resistance $R_{2s}$ across the $C_E$ terminals *(Fig. 3c)*. For the sake of simplicity, ignore the $R_{B1}$ and $R_{B2}$ resistances, because they are much larger than $R_S$. The resistance $R_{2s}$ is found by applying a test-voltage source at the emitter terminal of the transistor and measuring the resulting current:

$$I_T = \frac{V_T}{R_E} + \frac{V_T}{R_s + r_x + r_\pi} + V_T\frac{g_m r_\pi}{R_s + r_x + r_\pi} \qquad (9)$$

The first term in Equation 9 is current through the emitter resistor due to the voltage source; the second term is current through $R_S$, $r_x$, and $r_\pi$ due to the voltage source alone; and the third term is current due to the $g_m v_\pi$ generator. Recognizing that $g_m r_\pi = h_{fe}$, the resistance facing $C_E$ is given by:

$$R_{2s} = \frac{V_T}{I_T} = R_E \left\| \frac{R_s + r_x + r_\pi}{1 + h_{fe}} \right. \approx 18\ \Omega \qquad (10)$$



**2. THIS AMPLIFIER** is built with just one 2N3904 transistor, and has gain of greater than 100 for $\omega_L$ of less that 1 kHz.

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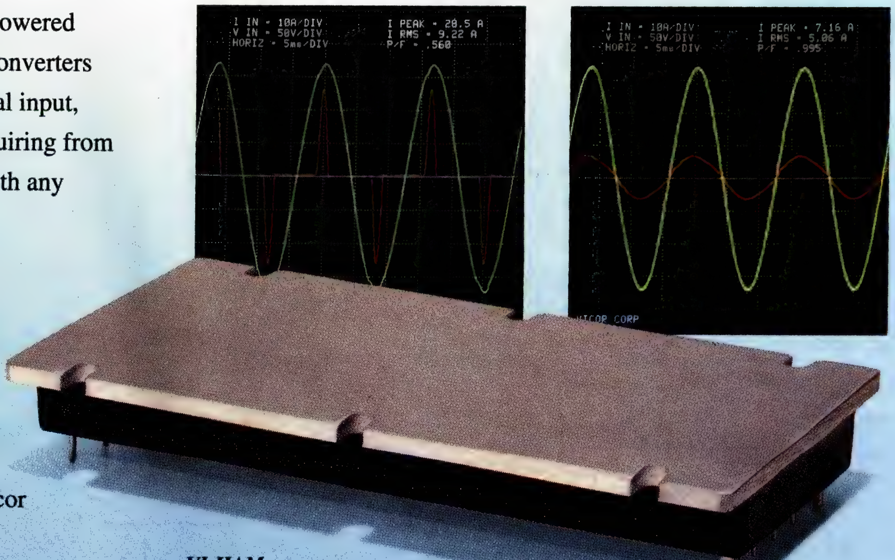

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Now, the final choice of capacitor values is constrained by Equation 7, which sets the minimum values of time constants $\tau_1$ and $\tau_2$. Arbitrarily "divide up" the time constants equally between the two capacitors.

$$\frac{1}{\tau_1} = \frac{1}{R_{1s}C_C} < 2\pi \times 500 \qquad (11)$$

$$\frac{1}{\tau_2} = \frac{1}{R_{2s}C_E} < 2\pi \times 500 \qquad (12)$$

This gives design values:

$$C_C > \frac{1}{2\pi \times 500 \times R_{1s}} > 0.09\ \mu F \qquad (13)$$

$$C_E > \frac{1}{2\pi \times 500 \times R_{2s}} > 18\ \mu F \qquad (14)$$

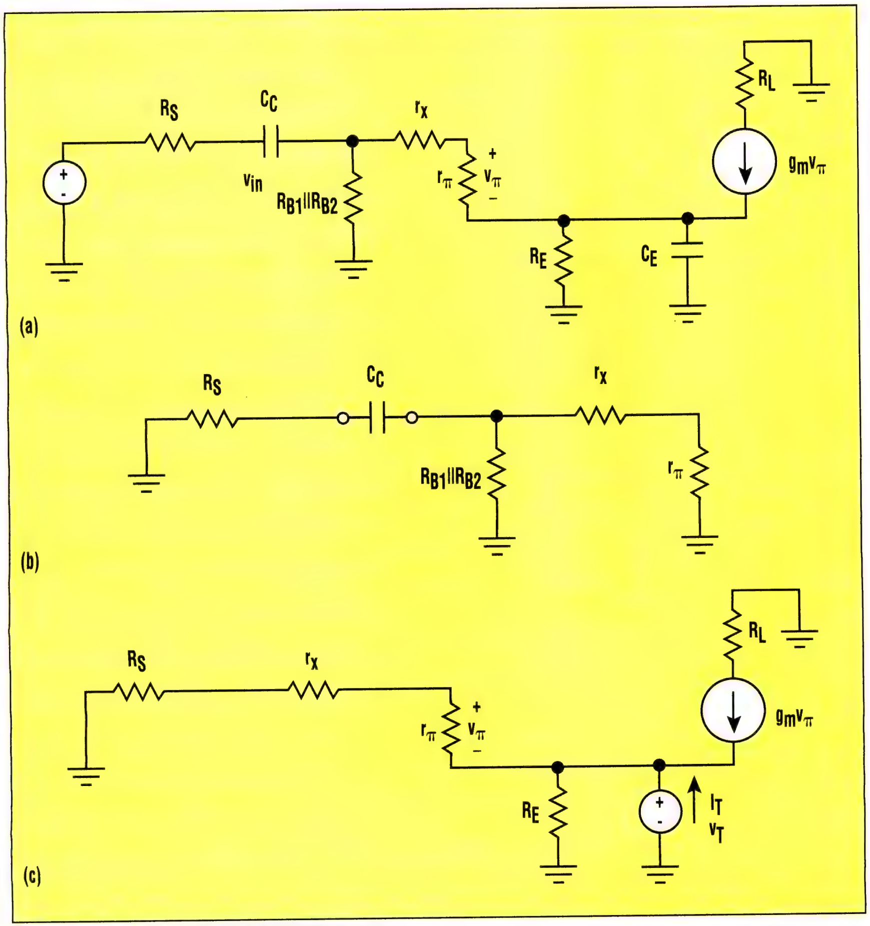
Chosen off-the-shelf values are $C_C = 0.1\ \mu F$, and $C_E = 20\ \mu F$.

The method of short-circuit time constants shows that a relatively small value of coupling capacitor $C_C$ will suffice due to the large resistance seen at its terminals. It also makes sense that $C_E$ must be a large capacitor value, because the output resistance of an emitter follower is very small.

## CAVEAT EMPTOR

It's obvious by inspecting Figure 2 that capacitors $C_C$ and $C_E$ affect the low- and mid-frequency behavior of the circuit. For instance, if capacitor $C_C$ were open-circuited, the mid-band gain of the amplifier would be zero. If capacitor $C_E$ were open-circuited, the mid-band gain of the amplifier would be about –2.

There are cases, however, where bypass capacitors have little or no effect on the mid-frequency performance of an amplifier. For instance, in a common-emitter amplifier with a cascode, the resistive network biasing the base of the cascode transistor is usually bypassed with a capacitor. The bypassing ensures better high-frequency performance, but has little effect at low and mid frequencies. This capacitor should not be included in the short-circuit time constants analysis. So, the moral is: think carefully about how the circuit operates before applying the short-circuit time constants method to a given capacitor in a circuit.



**3. THE LOW-FREQUENCY** model is used to calculate the short-circuit time constants (a). Shorting $C_C$ and $C_E$ helps determine the time constants $\tau_1$ and $\tau_2$, respectively (b,c).

## RESULTS

A Spice run shows that the gain of the circuit is approximately –110, with a low-frequency –3-dB point of 500 Hz. (Note that Spice was not used for design, only for verification). The answer obtained from using SCTC was not exact, but who cares? It's more important that engineers develop design insight by using such methods.

Short-circuit time constants offer guidance for choosing bypass- and coupling-capacitor values. Using this method, a design may be optimized for preferred capacitor values based on such criteria as size or cost. For instance, this article's design example divided up the time constant equally between the two capacitors, but any other combination will also work. As with the method of open-circuit time constants, all results are approximate. But the value of such methods is the design insight the method provides to the designers, not exact answers.☐

References:

Gray, Paul E., and Searle, Campbell L., *Electronic Principles Physics, Models, and Circuits.* John Wiley, 1967.

Thompson, Marc, "Design linear circuits using OCTC calculations," *Electronic Design Special Analog Issue*, June 24, 1993; p. 41.

*Marc Thompson is a senior engineer at Polaroid's Medical Imaging Systems. He has BS and MS degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, and is currently pursuing his PhD.*

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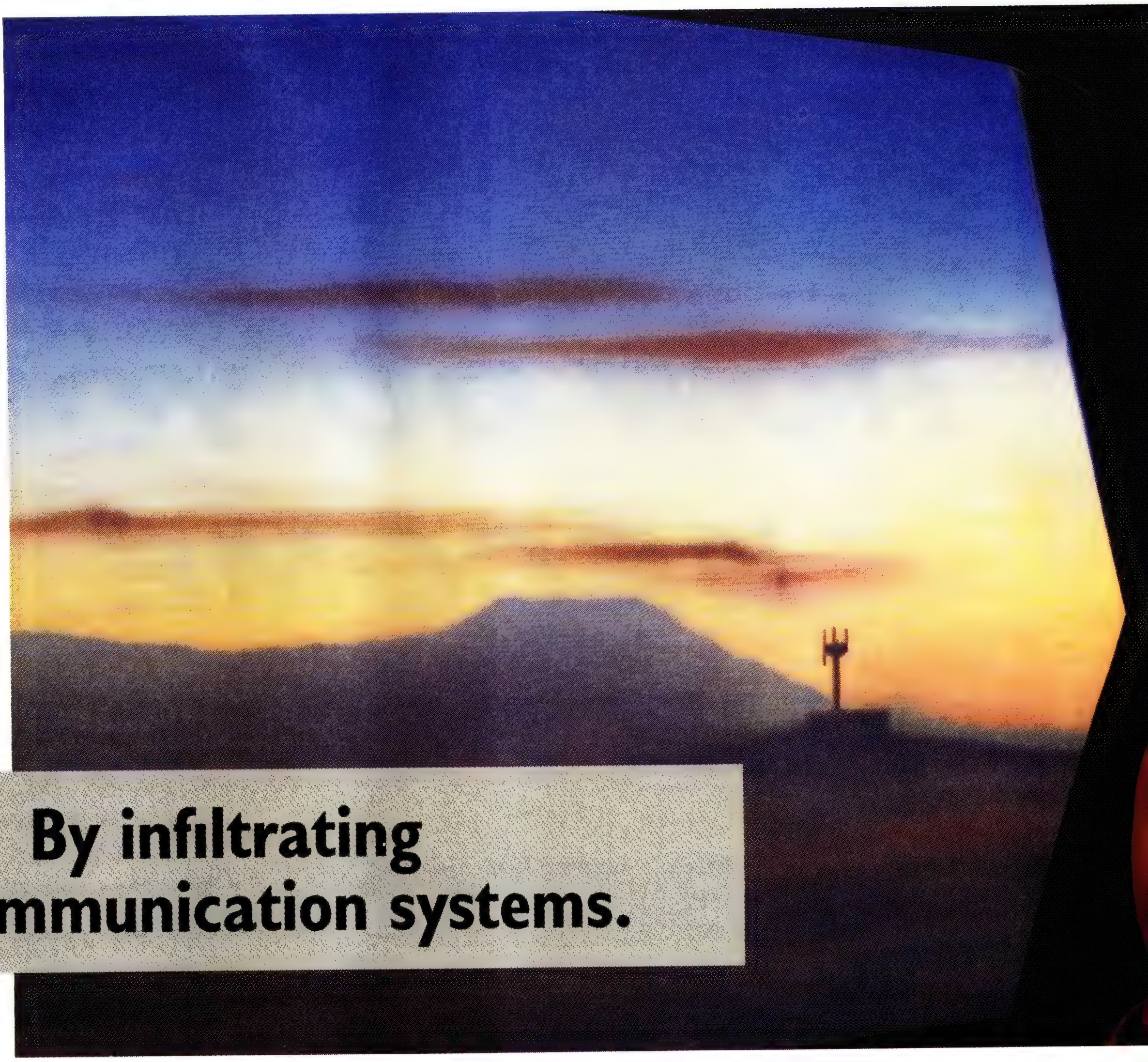

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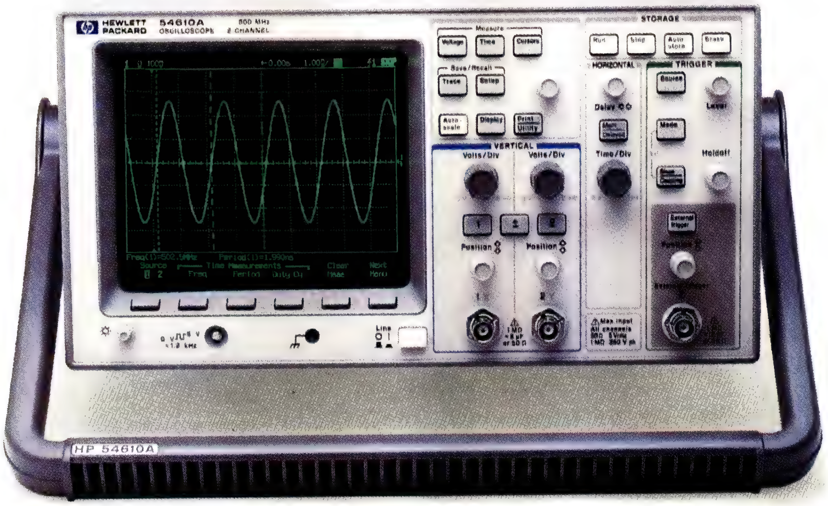

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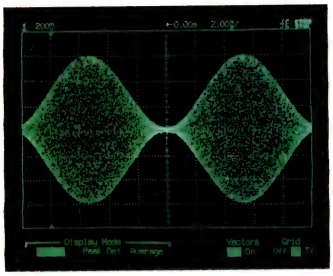

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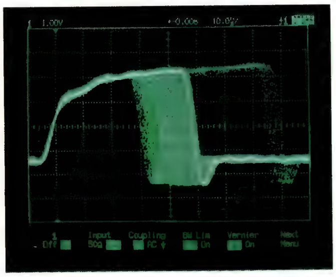

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**CIRCLE 521**

# CREATE EFFICIENT LASER POWER SUPPLY

JIM WILLIAMS
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035-7487.

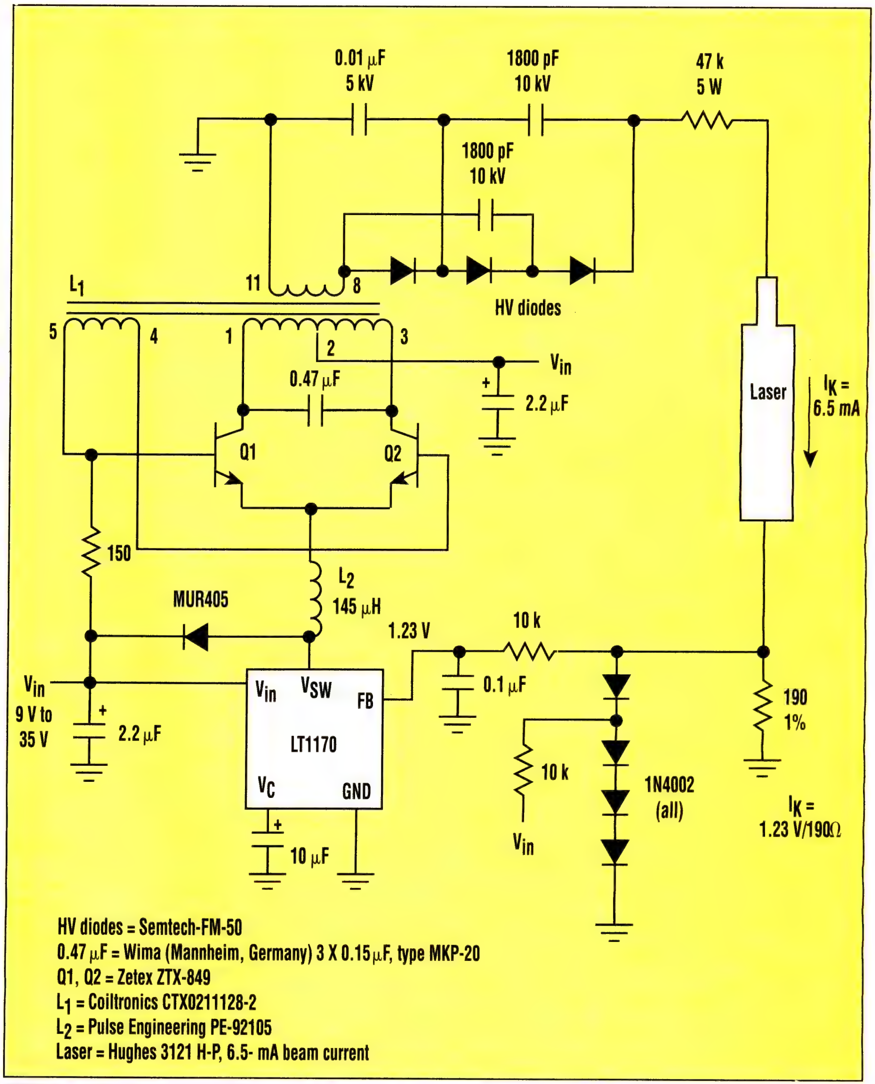
Helium-neon lasers are useful in a variety of tasks, but they're difficult loads for a power supply to handle. Powering a laser usually involves some form of startup circuitry to generate the initial breakdown voltage and a separate supply to sustain conduction. Typically, almost 10 kV is needed to start conduction, and about 1500 V is required to maintain conduction at their specified operating current.The circuit shown considerably simplifies driving the laser *(see the figure)*. The startup and sustaining functions are combined into a single closed-loop current source with over 10 kV of compliance.

When power is applied, the laser doesn't conduct and the voltage across the 190-Ω resistor is zero, and the LT1170 switching-regulator "FB" pin observes no feedback voltage. Therefore its switch pin ($V_{SW}$) provides full duty-cycle pulse-width modulation to $L_2$. Current flows from $L_1$'s center tap through Q1 and Q2 into $L_2$ and the LT1170. This flow causes Q1 and Q2 to switch, alternately driving $L_1$.

When the 0.47-μF capacitor resonates with $L_1$, it supplies boosted sine-wave drive. $L_1$ provides substantial step-up, which causes about 3500 V to appear at its secondary. The capacitors associated with $L_1$'s secondary form a voltage tripler, producing over 10 kV across the laser. The laser breaks down and current begins to flow through it.

The 47-kΩ resistor ballasts the laser, which limits current. That current flow causes a voltage to appear across the 190-Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin and subsequently closes a control loop. The LT1170 adjusts its pulse-width drive to $L_2$ to maintain the FB pin at 1.23 V, regardless of changes in operating conditions. The laser can then see constant current drive, which in this case is 6.5 mA. Other currents are obtainable by varying the 190-Ω value.

The 1N4002 diode string clamps the voltage when laser conduction begins, protecting the LT1170. The 10-μF capacitor at the $V_C$ pin frequency compensates the loop. The MUR405 maintains $L_2$'s current when the $V_{SW}$ pin isn't conducting. The circuit starts and runs the laser over a 9-to-35-V input range with about 75% electrical efficiency.☐



HV diodes = Semtech-FM-50
0.47 μF = Wima (Mannheim, Germany) 3 X 0.15μF, type MKP-20
Q1, Q2 = Zetex ZTX-849
$L_1$ = Coiltronics CTX0211128-2
$L_2$ = Pulse Engineering PE-92105
Laser = Hughes 3121 H-P, 6.5- mA beam current

**DRIVING HELIUM-NEON LASERS** can be simplified considerably using this power-supply configuration. When power is applied, the laser doesn't conduct and the voltage across the 190-Ω resistor is zero. However, a resonant circuit and a voltage tripler then produce over 10kV to turn on the laser.

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CIRCLE 522

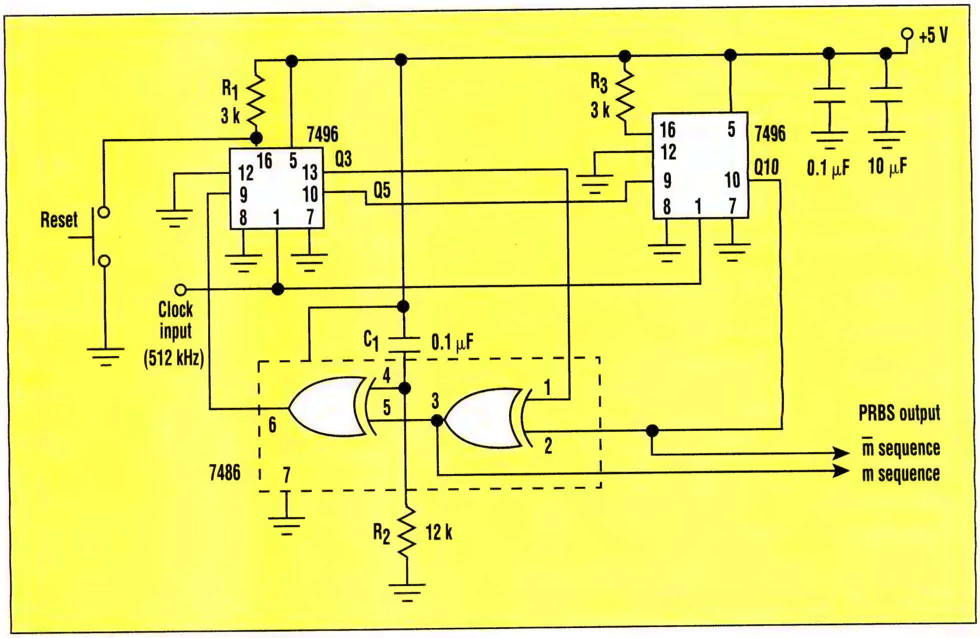
# PRBS GENERATOR SELF-STARTS

BRIAN BREWSTER
Satellite Microwave & Communications Ltd., Postbus 10416, 6000GK Weert, The Netherlands.

Pseudo-random bit sequences (PRBSs) are widely employed in various applications, such as test sources, noise generators, and scrambling and spread-spectrum systems. A common implementation is to employ an n-stage shift register with modulo-2 feedback at m taps to generate a maximum length sequence $2^n - 1$. These sequences will cycle through all n-bit states with the exception of the all-zero state. Therefore, at power initialization, the shift register will remain in a static condition, because $0 \oplus 0 = 0$, where $\oplus$ denotes the exclusive-OR operator. As a result, additional logic is required to inject at least one logic 1 bit into the shift register at power startup.

In this circuit *(see the figure)*, an additional exclusive-OR gate is connected after the modulo-2 feedback, with $C_1$ and $R_2$ applying the supply turn-on ramp into the feedback loop. This provides sufficient transient signal so that the PRBS generator can self-start at power-up. A shift-register length n of 10 is shown with feedback at stages 3 and 10, providing true and inverted maximal length sequence outputs.

This technique applies an input directly to the feedback loop. Therefore, it's considered more reliable than applying an RC configuration to the shift-register reset input to create a random turn-on state.☐



**ADDING AN EXCLUSIVE-OR GATE** to a PBRS generator provides the generator with sufficient transient signal so that it can self-start at power-up.

## IFD WINNERS

### IFD Winner for May 27, 1993

**Mike Grimm,** Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086; (408) 737-7600. His idea: *"Isolated, Regulated 5V from AC line."*

### IFD Winner for June 10, 1993

**Clive Bolton and Pace Willisson,** Bolton Engineering Inc., 37 Washington Street, Melrose, MA 02176 and Blitz Product Developement Corp., 4 Spruce Road, Medway, MA 02053, respectively. Their idea: *"Extend The Range of RS485 Networks."*

CIRCLE 523

# GENERATING SINE WAVEFORMS

YONGPING XIA
EBT Inc., 2522 W. 237th St., Torrance, CA 90505.

A square waveform filtered by a high-order low-pass filter in which –3-dB frequency is lower than signal frequency will eliminate most harmonics of the waveform. As a result, the filter outputs a fundamental sine waveform. This method is applied to generate a sine waveform by using a switched-capacitor filter (MAX292) *(see the figure)*. This circuit offers wide frequency range (0.1 Hz to 25 kHz), low distortion, and constant output amplitude in the whole frequency range.

MAX292 (IC2) is an 8th-order low-pass Bessel filter. Its –3-dB corner frequency is determined by its clock frequency divided by 100. In other words, the corner frequency is 1 kHz if the clock 100 kHz. IC1 (74HC4060) is a 14-bit binary counter with a built-in oscillator. Its Q4 generates IC2's clock and Q10 sends a square waveform as IC2's input. Because the frequency ratio of the clock and input is 64:1 (which is lower than the –3-dB ratio), only the square waveform's

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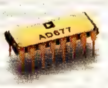

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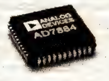

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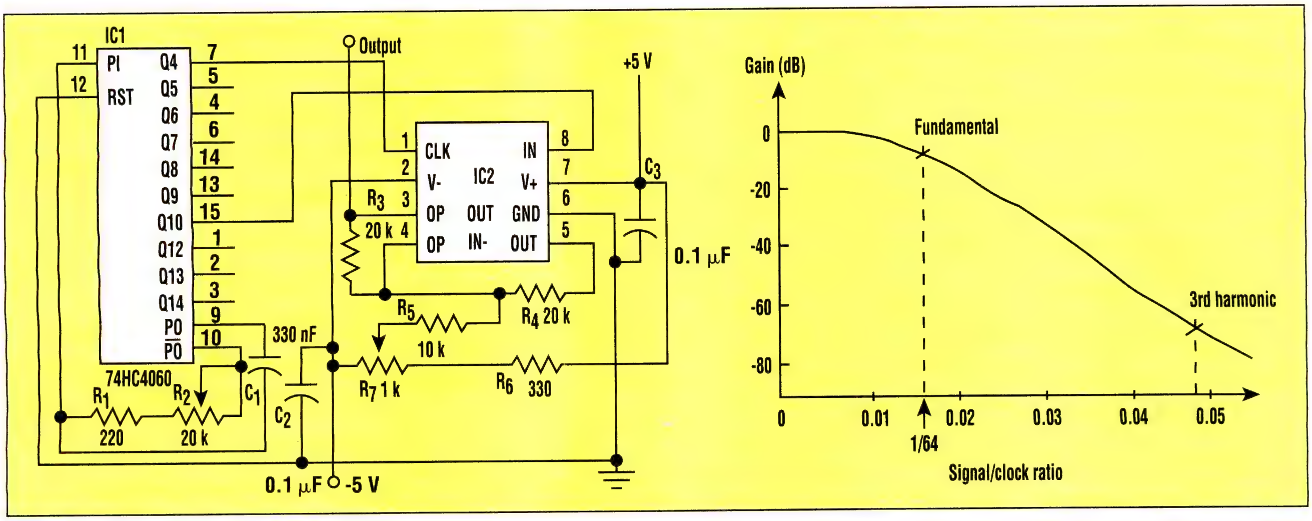
fundamental can partially pass through the filter, with about 9-dB loss. The third harmonic will be down about 65 dB.

Thus, the filter outputs a pure sine waveform with approximately a 2.5-V p-p amplitude. Because the ratio is a constant, output amplitude will also be constant throughout the entire frequency range. IC2 contains an uncommitted op amp that's used to offset output dc level by adjusting resistor $R_7$.

$R_1$, $R_2$, and $C_1$ determine IC1 oscillation frequency, which is 16 times the output frequency. Useful output-frequency range is from 0.1 Hz to 25 kHz. By using the component values in the figure, it's possible to achieve a frequency range of 80 Hz to 7.5 kHz.☐



**A PURE SINE WAVEFORM** can be generated with this circuit, which employs a switched-capacitor filter. Other key attributes are wide frequency range, low distortion, and constant output amplitude throughout the entire frequency range.

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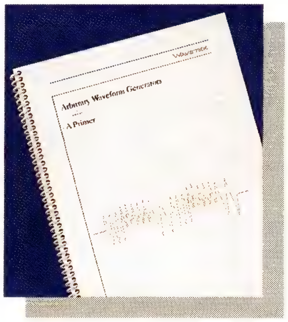

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# QUICK LOOK

EDITED BY SHERRIE VAN TYLE

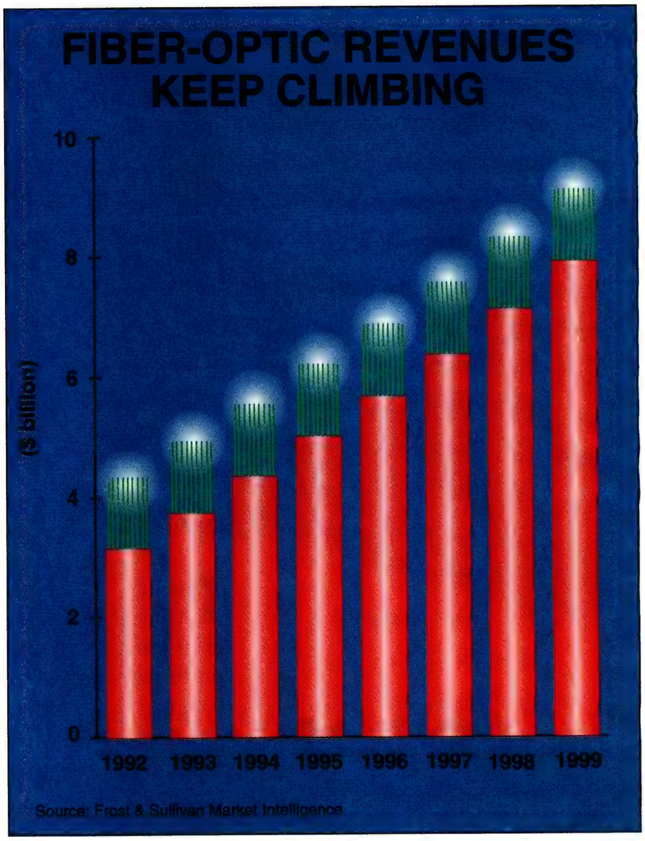
## MARKET FACTS

Propelled by demand for fiber in local area networks and local exchange networks, the worldwide market for fiber-optic communications is expected to more than double from $4.4 billion last year to $9.1 billion by 1999, growing at an 11% compound annual rate. That's the prediction of Frost & Sullivan Market Intelligence in a recent report, World Fiber Optic Communication Markets.

Revenues for cable will dip in comparison to sales of transmitters, receivers, and interconnection devices, according to the Mountain View, Calif., market researchers. Cable's share of total market revenues will drop from 59% last year to 44% by 1999 while receivers will rise from 9% to 17% in the same period as new technologies enable sharing of more receivers by common transmitters. Transmitters will expand in share from 24% to 27% of the market; connectors from 6% to 8%; and couplers from 3% to 4%.

Installed at first mostly in U. S. long-distance networks, which are now largely completed, fiber is being installed on international transmission and local area networks and local exchange networks.

Although North America accounted for 48% of last year's sales, that share will decline to just over 40% by 1999 as the Pacific Rim's market share grows from 21% to 25% of global fiber demand and Europe's portion increases from 20% to 23%. Optoelectronic ICs, still in early development, will be a low-cost alternative to today's components in increasing system performance. The optical fiber amplifier is a likely replacement for expensive electronic regenerators in long-distance systems, predicts Frost & Sullivan Market Intelligence.


FIBER-OPTIC REVENUES KEEP CLIMBING

Source: Frost & Sullivan Market Intelligence

## BEST SELLERS

What are the best-selling books in electronics and computer science?

**ELECTRONICS**

**1.** *Art of Electronics*, 2nd ed. by Paul Horowitz and Winfield Hill. Cambridge University Press, 1990. $59.95.

**2.** *Art of Electronics Student Manual* by Paul Horowitz. Cambridge University Press, 1992. $27.95.

**3.** *Basic Electronics*, 7th ed. by Bernard Grob. Glencoe, 1992. $47.95.

**4.** *JPEG Still Image Data Compression* by William Pennebaker. Van Nostrand Rinehold, 1992. $59.95.

**COMPUTER SCIENCE**

**1.** *TCP/IP Network Administration* by Craig Hunt. O'Reilly & Associates, 1992. $29.95.

**2.** *Nanosystems Molecular Machinery* by Eric Drexler. John Wiley & Sons, 1992. $24.95.

**3.** *Cyberarts* by Linda Jacobsen. Publisher's Group West, 1992. $22.95.

**4.** *Nanotechnology Research* by B.C. Crandall. MIT Press, 1993. $39.95.

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax -0693

## QUICK NEWS: SEMINARS

GeoWorks, creator of the Geos operating system, hosts a software developers conference Oct. 25-26 at the Hyatt Regency in Burlingame, Calif. Cost is $445 for early bird registrants; $595 after Oct. 6. Contact GeoWorks, 2150 Shattuck Ave., Berkeley, CA 94704; (800) 524-1857, ext. 1214; (510) 644-0883; fax -0928. CIRCLE 481

The University of Wisconsin is offering an audio-graphics course—design and application of electrical contacts (program A067)—Oct. 4-21, 1993. Contact the Department of Engineering Professional Development, University of Wisconsin—Madison, 432 North Lake St., Madison, WI 53706; (800) 462-0876; fax (608) 263-3160. CIRCLE 482

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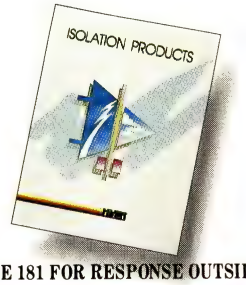
- **ISO212**—a low cost, differential input, differential output, 750Vrms isolation amp with an internal, isolated DC/DC converter
- **3656**—a transformer-coupled amp with an internal, isolated DC/DC converter that offers three port isolation



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## OFFERS YOU CAN'T REFUSE

Robochart is a mouse-driven flow diagram editor that runs under Solaris 2.x. An evaluation package of Robochart, containing the full program with file saving disabled, is $25, which is refundable with the purchase of a license. Contact Digital Insight, P. O. Box 533, Simi Valley, CA 93062-0533; (805) 583-3627; fax -3809. CIRCLE 483

A free information disk gives an overview of Eagle pc-board software. A slide show introduces the program's main features and answers the most common questions asked about Eagle. Contact CadSoft Computer Inc., 801 South Federal Highway, Delray Beach, FL 33483; (407) 274-8355; fax -8218. CIRCLE 484

A preview of a three-tape course on the cooling of electronic equipment is $25 for shipping and handling. The complete course, which is $395, covers all cooling methods. Design formulas for making calculations with particular cooling methods are presented. Tables of thermal properties of materials are given. Exercises involving actual equipment are assigned. Solutions are presented at the beginning of the next session. The shipping and handling charge can be applied to the course purchase. Contact Scott Training Associates, 101 First St., Suite 393, Los Altos, CA 94022. CIRCLE 485

A demo disk is free for ControlWare, a tool for designing, analyzing, and simulating dynamic systems and feedback controllers on Macintosh PCs. Users can work quickly without sacrificing power or capability. ControlWare has a full set of simulation features, including linear and nonlinear modeling blocks, signal generators, plotters, logic blocks, and hierarchical and custom blocks. Contact Seagull Technology Inc., 1310 Hollenbeck Ave., Suite F, Sunnyvale, CA 94087; (408) 732-9620; fax (408) 736-7103. CIRCLE 486

A buyer's guide for Unix and client/server computing includes programming tools, object-oriented class libraries, voice-recognition/macro building programs, network management tools and project-management software. Contact the Qualix Group Inc., 1900 S. Norfolk St., Suite 224, San Mateo, CA 94403; (800) 245-8649 or (415) 572-0200; fax -1300; e-mail: info@. CIRCLE 487

## QUICK NEWS

Speedy delivery of data sheets and literature about Micron Semiconductor's products is afforded by a fax-on-demand system from the Boise, Idaho, company. The system uses FactsLine software from IBEX Technologies, Placerville, Calif., which enables users to listen to a voice menu, select documents or an index with the fax/phone keypad, and receive the information by fax. Data Fax may be accessed by dialing (208) 368-5800. Micron is located at 2805 East Columbia Rd., Boise, ID 83706-9698. CIRCLE 488

The National Institute of Standards is asking for comments on its plan to harmonize U. S. lab accreditation to international standards. For information, contact Albert Tholen, chief, National Voluntary Laboratory Accreditation Program, A162, Bldg. 411, NIST, Gaithersburg, MD 20899-0001; (301) 975-4016; fax 926-2884. Written comments are due by Oct. 11, 1993.

## KMET'S KORNER

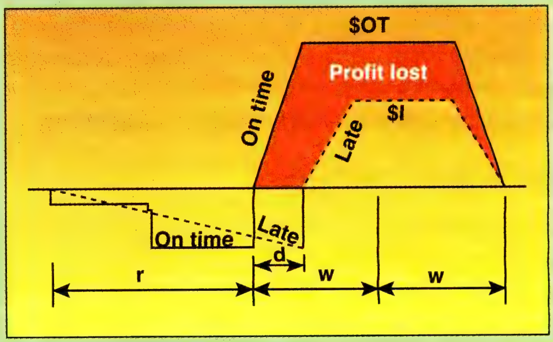
# ...Perspectives on Time-to-Market

**BY RON KMETOVICZ**
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

The illustration in this column forms the visual link between investment and profits. And it connects many of the interactive items discussed in previous columns. The model helps you see how using the speed staffing profile makes you a financial winner.

The "on time" monthly expenditure of cash follows the speed staffing profile discussed in previous columns. This profile makes it evident that the development effort went through a complete definition phase that was followed by a short, but detailed, planning phase before executing the new product development effort. Total development costs for the effort are obtained by finding the area under the curve.

The "late" engineering profile is represented by a triangle. Total expenses, as computed by finding the area under the curve, for this profile are drawn to be about equal to the "on time" profile. Setting the areas under the curves to equal each other is a scenario that is generous toward the "ramp" profile. As described, it is not unusual to have new product development efforts that take longer cost more. This triangular expense profile is typical of projects that tend to have delayed market entry. In this case, "on time" development time "r" is extended by "d". Total development time then becomes "r + d" in duration as the product enters the market well into its market window, "w".



For discussion purposes, the assumption is made that either one of these profiles is possible for the new product under development. This assumption then makes it possible to explore the product's revenue generation potential as a function of its market entry delay.

The investment profiles are then connected to the revenue profiles at the appropriate point. Use of the speed profile supports the generation of maximum life-time profit. Late market entry reduces returns. Visualization of how parameters interact should now be in place and ready for further study.

Do you have the big financial picture?

*More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.*

# QUICKLOOK

## DID YOU KNOW?

. . . that last year U. S. electronics firms boosted turnover of their inventory to an all time high of 5.17 turns, up from 4.65 the year before. In contrast, a decade ago inventory turnover was 2.91. In terms of dollars, five turns a year means that a $1 billion company requires about $100 million less inventory.

A survey of 70 electronics companies by consultants Pittiglio Rabin Todd & McBrath, of Weston, Ma.; (617) 647-2800

## TALES FROM A SKUNK WORKS

My last column drew a real-world example from the airline industry showing total team commitment. Today, U. S. companies are competing with committed, empowered teams around the world. For this reason, many firms are losing, and that's why we need skunk works.

I had the opportunity to contrast this case with typical Western practices. I gave a lecture on a computer network and was given guest privileges to browse the various forums. I blundered into a debate on the shame of how hard it was to make any scientific and technical progress in the midst of hostility and litigation: "Kill the lawyers! It's all their fault."

My comment was, "Hey people, what of truly outrageous acts? For example, consider those living downwind of the Hanford (Wash.) nuclear power plant who were damaged by years of dumping radioactive materials into their air and drinking water?" I suggested that such rude acts might prompt litigation. According to the March 15, 1993 *Oregonian,* 585,000 curies were released in 1945 and tens of thousand of curies were released per day into the Columbia River from 1944 through the early 70s. Three Mile Island, by comparison, released only 15 curies.

What I didn't know was that the sysop for that forum had worked at Hanford for 15 years. His responses seemed testy and defensive. After we got through the denial stage, his core defense was that no laws were broken and no one could *prove* that their specific cancer was related to a specific radiation release decades before. It's the "tobacco defense" and technically true.

This got me thinking of the contrast between the Japan Air Lines crash (see my Sept. 2 column) and the Hanford incidents. In the JAL case the company as a team clearly did all in its power to apologize and to correct the harm it had done. The airline did not quibble, split hairs, or force the victims to prove anything. Those responsible made extreme acts of atonement, and, most important, the incident was resolved without litigation and in a way that restored trust.

The Hanford case is a classic U. S. legal conflict. The victims are accused of ignorance and greed. Incredibly detailed and complex "proof" is demanded at every level on every sub-issue. Hostility is high; trust is nonexistent; so litigation and gridlock result.

The contrast between Western justice and Japanese self-enforcement of trust is interesting. Which society would tend to have the most litigation? Which would find it easier to do products and make scientific progress? Which would adapt better to change?

Anyway, effective skunk works *cannot* exist in an environment of micro-management, procedures, and proof. Creativity and risk taking quickly vanish without mutual trust and commitment.

Instead of power, boxes, and turf, the new values are shared vision, teams, and results. Instead of breaking work into minimum skills and small pieces, try forming the best people with broad skills (including "outsiders" and consultants) into self-managing teams. Move your thinking from crisis to outcomes. You will be pleasantly surprised at what your skunk works can achieve.

*John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of* High Tech with Low Risk. *To order, phone (503) 280-8547.*

## HOT PC PRODUCTS

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CIRCLE 489

Some cache and disk compression programs damage files or entire disks. To ensure that programs and data remain unharmed, programs such as Integrity Master enable users to take advantage of disk compression, disk cache, and other resident software by checking all files and system sectors for changes. Each change is analyzed and (optionally) reported. The program does not just spot check but reads every byte. Integrity Master can be used out of the box, its maker says; onscreen menus and context-sensitive help are available. List price is $35. An evaluation version is available on many bulletin board systems (BBS), on-line systems, and shareware disk vendors. Contact Stiller Research, 2625 Ridgeway St., Tallahassee, FL 32310-5169; (800) 788-0787; (314) 256-3130; fax 966-1833.

CIRCLE 490

## QUICK REVIEWS

*Software Engineering and CASE: Bridging the Culture Gap,* by Tom Fletcher and Jim Hunt, guides readers through implementing CASE and software engineering from the top down. Rather than a quick fix (getting to the code as quickly as possible), the chapters build an infrastructure—complete with methods, procedures, tools, and a supportive culture. The book devotes a chapter to the change process, including how to deal with resistance. An appendix contains forms for SE/CASE assessment. The $40 book is published by McGraw-Hill in the CAP Gemini America series (ISBN 0-07-021219-8); (800) 822-8158.

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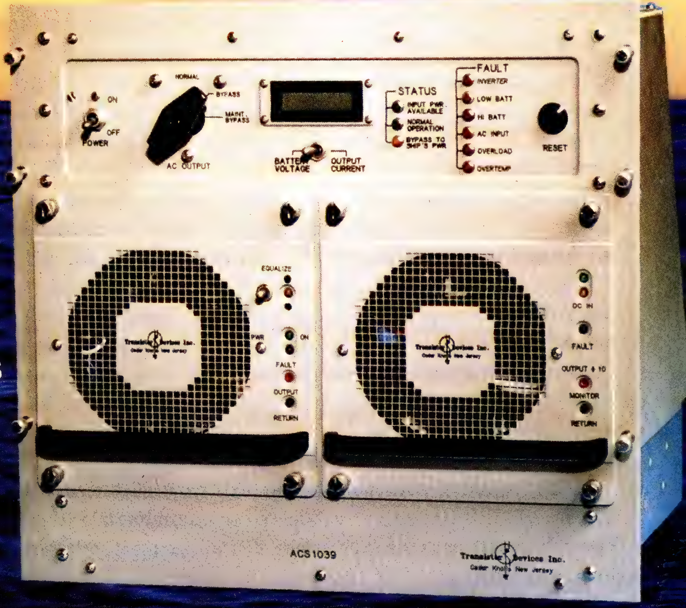

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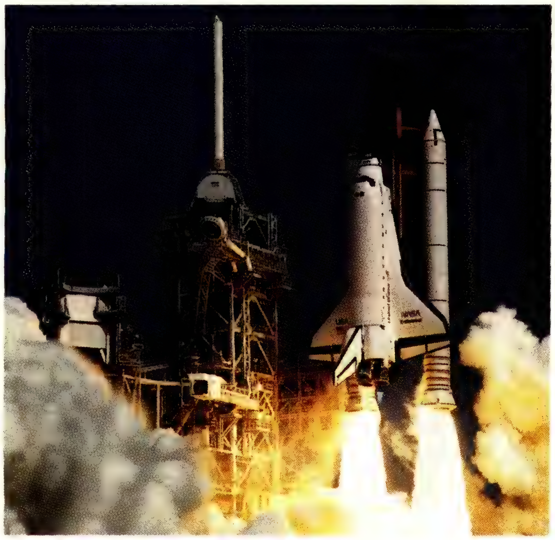

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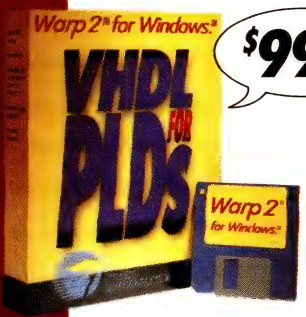

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## PEASE PORRIDGE

# WHAT'S ALL THIS ESD STUFF, ANYHOW?

Recently a guy asked me to present a lecture to the Silicon Valley ESD Society—a lecture about ElectroStatic Discharge. That's a little like bringing coals to Newcastle—what the heck could I tell *them* that they did not already know? I did know how I would start out. But after the beginning, then what? And if I wrote down everything I told them, would that make a useful, valuable column? Let's see....

First I told them about the ESD newsletter we started at National a few years ago. The purpose was to inform all of the engineers of new developments so we could meet high levels of ESD on our new ICs with a minimum amount of wasted effort. Jolly good. Shortly after that, the editors posted a list of the ICs that would survive a very high ESD rating. We were exhorted to go out and learn how these engineers got such good ESD ratings. Two of the best three were digital ICs, so all of our analog engineers were encouraged to learn the secrets of that one "robust" analog circuit that would pass not just 2 kV, or 4, but 6 kV of ESD. Hey, that's really a very good, strong ESD circuit. How did those designers do it? With a special ESD protection algorithm and special clamp diodes? Let's find out what this circuit looks like!

**BOB PEASE** OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

First, what's the name of this IC? It's an LM340. Okay—do you guys recognize the part number? The LM340 is a 1-A, 3-terminal regulator, and for all intents and practical purposes, it passes a high ESD test by the *brilliant strategy* of having a 1-A power transistor on every pin. So, if we want to design a quad op amp with really good ESD ratings, obviously all we have to do is add twelve 1-A power transistors, one on each input and output pin. Of course, the die size of an LM324 would increase by a factor of 9, and the input capacitance and leakage would be completely unacceptable. Everybody would love the ESD ratings, but nobody could afford the circuit. In fact, we could not even fit it into a 14-pin DIP package. But if we're to learn from the LM340's designer (George Cleveland) and if we applied his teaching so as to achieve the *highest* ESD ratings, then that's the circuit we would design. Ahem. Ahem! Needless to say, we came up with some slightly more *compact* and *cost-effective* circuits to protect our new ICs.

Similarly, one of our customers wanted to see our report on ESD on a new IC. It passed the required 2-kV test on 37 of the 40 pins. So the customer proposed that we must add a new ESD cell to *all* of the pins to improve the ESD ratings. After all, the customer wanted the *highest possible* ratings. But we observed that if we add the ESD cell to every pin, the die size would increase by 12%, the yield would drop, and the cost per IC would increase by several percentage points. If they wanted to have the highest ESD tolerance, did they want to pay for it? No. So, after much debate, they decided to accept the part with the ESD cell added to only those pins that needed it. *That* was what they were willing to pay for.

Now, most people have an adequate awareness of ESD problems. If you walk across a carpet on a dry day in winter and bring your finger near a circuit, it's real easy to generate a spark that might damage the circuit. The industry has a reasonably accurate model of this abuse: Charge up a 100-pF capacitor to a couple thousand volts, and then discharge the capacitor through a 1500-Ω resistor into a pin or node of a circuit. This impedance is commonly known as the "human body model." This is considered a fairly minimal ESD test, yet it puts a surge of 1.3 A through most paths for a couple hundred nanoseconds. That's pretty scary for a little IC where the data sheet tells you to never exceed 10 mA into any pin. A lot of good ICs will

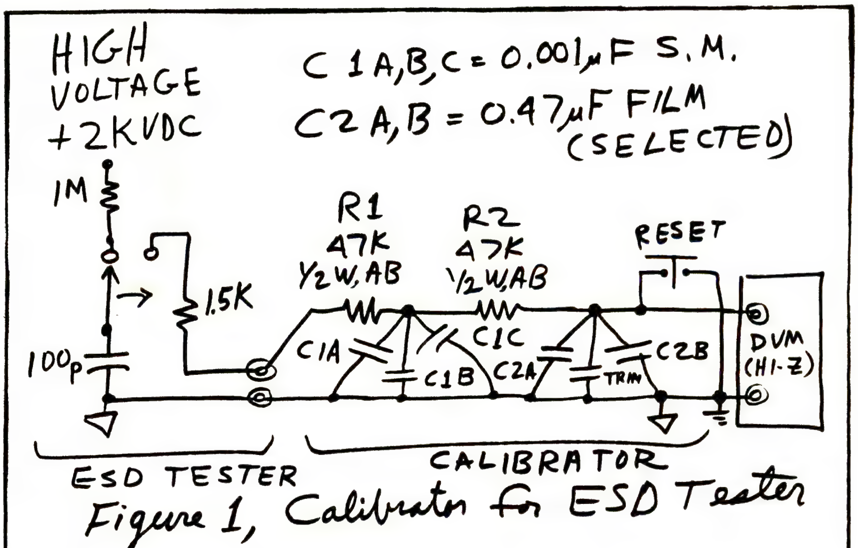


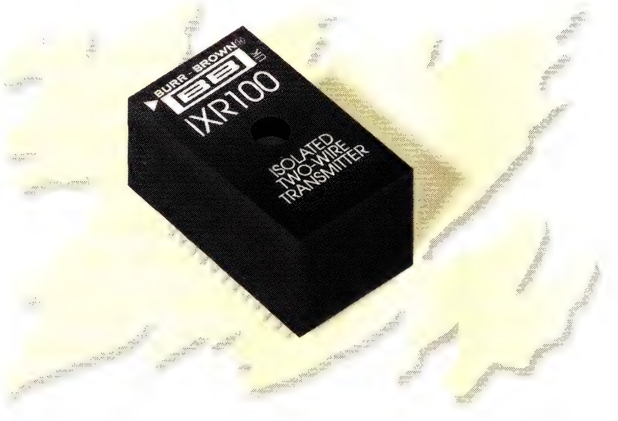
Figure 1, Calibrator for ESD Tester

pass this test, and even if the voltage is doubled, (note also that the energy will quadruple) some ICs survive just fine. But a lot of them do not. So if you are building a million radios, there's a definite incentive to buy semiconductors that are pretty reliable. Minor accidents that cause an occasional zap to a circuit may occur even though every assembler or worker on the production line is carefully grounded through a 1-MΩ wrist strap.

Now, when is a piece of "grounded" test equipment not "grounded?" When you can measure 500 V on some parts of the equipment, for example. (Once I saw a lab where two workbenches, about 7 feet apart, had 2500-V ac between them...a long time ago.) When is a 1-MΩ floor not 1 MΩ? When the janitor decided to wax it... What is the main difference between a conveyor belt on a production line, and one on a Van de Graaff generator? Answer, one is vertical and the other is horizontal. But both can generate lots of volts.

So, to make sure our ICs are reliable, we have bought various ESD testers, and we perform all sorts of zap tests on our new *and* old ICs. I once wanted to add a Zener diode to a pin of one of my ICs to prevent damage to a differential pair. One of the senior engineers said, when he saw my drawing, "You'll get in trouble when that Zener gets zapped by ESD." But after a lot of thought, I left it in anyway, and in actuality, we have never had any customer complaints about that terminal. I checked recently, and that IC has passed 2000 V on every pin—even the pin with the Zener. So when an expert tells you, "You have to do *this*, and you can't do *that*," just remember that even experts can be wrong....

One major purchaser of ICs came out with a drawing for the "Machine Model" of ESD testing. This represents what happens when a device is held in a large metal arm, inadvertently charged to a high voltage, and then it touches a grounded piece of metal. In this test, a 100-pF capacitor is discharged through 0 Ω (not 1500 Ω) into a device's pin. Well, if you could really discharge a capacitor through 0 Ω, the current would be infinite, right? Ah, but there's always some inductance. And if you stand at the DUT and look back at the capacitance, the wiring has a certain characteristic impedance or resistance—perhaps 50 Ω, perhaps 90 Ω. That helps explain why you can't have an infinite current, and you can't have 0 Ω. After several suppliers complained to the Customer that it wasn't realistic to have a source impedance of 0 Ω for that test, the Customer changed the control drawing to say "0 Ω ±5%." Still, despite cases as silly as that, it's important when you do your ESD testing to keep your wires fairly short and compact,



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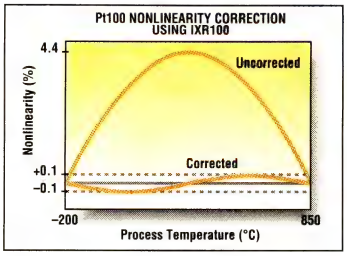

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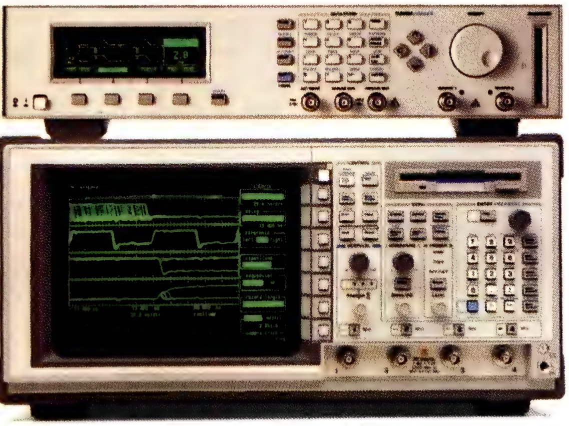

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to keep the inductance low. This gives a fair rise time for the current pulse. No point in trying to fool everybody, including yourself, with a wiring path that causes slow rise times.

National bought a $200,000 Zap-Master ESD tester from Keytek*—there are only two in the world (AT&T has the other one). When we test parts and get results, they don't agree with AT&T's results. That's because AT&T chose to use their machine to apply pulses, both + and –, into a grounded part. NSC chose to apply a high voltage bias to the DUT and discharge the part into ground, which is a more severe test. It just goes to show that there are many disagreements on what is the "right" way to do an ESD test. There isn't necessarily any fully-agreed-upon procedure, no "industry standard," no repeatable test, no consistent results. However, we've been able to use some of these tests to design ESD structures that not only meet good ESD ratings, but are also predictable by Spice analysis. So if Spice can teach us what is *good*, maybe it can teach us what is *better*. If we are able to come out with consistently improved stress ratings in a year or two, I will be impressed, and amazed!!

What happens when one IC of a lot of 30 fails at 1300 V, and the other 29 survive past 2300 V? That's very frustrating, and it may indicate a minor manufacturing flaw (a pin-hole oxide flaw?) that happens at a low occurrence rate. Sometimes you get 11 out of 30 failing at 1300 V and 19 good at 2300 V. Very confusing. One guy pointed out that this can happen when some of the gates and flip-flops start up in one output state, which is more resistant to stress. If the gates bias up to the opposite state on another pulse, the part might fail. So, sometimes you can test a part five times at 1600 V and it's okay, yet the next test at 1200 V causes a failure. Does it sound to you like there's something nonlinear going on??!! Well, if you think it's fun to analyze circuits in Spice at audio frequencies, just imagine how much fun it is to analyze the transient response of a little piece of an IC, where the current builds up to a couple amperes in 10 ns! Some engineers, though, seem to be making some progress in this area.

But what if you test a batch of ICs and they're all passing 2400 V just fine, yet you take them over to another tester and they start failing at 1400 V? Does that mean that the first half of the batch of ICs is much stronger than the second half? No, that's not the case. That dichotomy usually occurs because the *second* ESD tester—the one that belongs to the Reliability Group—is well calibrated. The problem arises because the *first* tester, which is kept around the development engineering lab, has gone out of calibration and is putting out MUCH too low a pulse. Thus, the parts are made to look good due to false testing. Let me assure you, I've heard of this happening several times. In fact, a guy told me yesterday that it happened *again* to his newest IC. His initial test led him to think it was okay, but the accurate tester told him that it really was not. We were fooled, but not for long.

I told him to go out and make up a calibrator network to add onto the ESD tester. The network is really very simple, as shown in Figure 1. The exact R and C values aren't important, but you really do want to understand the philosophy. Every time you "hit the button" to discharge the capacitor, a certain quantity of charge ($Q = C \times V$) is dumped down into the big capacitors. If the total capacitance is about 1 µF, then 200-mV output change corresponds to 2 kV of ESD pulse. So the main thing is to have C2 at about 1.0 µF. I like to make C2 out of a couple selected 0.47 µF caps. Why selected? Well, if the first two capacitors I grabbed were 0.52 µF, the calibration factor would be off, and it would be hard to trim to get the right scale factor. So the selection process is to select 2 or 3 capacitors that make up 0.95 to 0.99 µF total. Then add on some trim caps to get the total near 0.997 µF. That covers the calibration.

Why bother to have C1? Well, if you force a 2-A pulse into a wound film capacitor, the inductance of the windings might cause a voltage overstress of the film. It's better to have C1 = 3000 pF so that the pulse of current fed to C2 doesn't have any extreme values. The other good thing about C1 is making it out of three 1000-pF capacitors, perhaps NP0 ceramic or silvered mica, that are standing up like a tripod. Then, if you make C2 out of two film capacitors that act like a bipod, the whole scheme stands up off a little piece of copper-clad fairly strong and rigid, not wobbly as it would be if you just used one capacitor for C1 and one for C2.

What about R1? Well, I would use 47 k or 47 Ω, carbon composition, Allen Bradley 1/2 watt. The resistance value is not a big deal, but you really should use a carbon-composition type that can handle an ampere or two without breaking down (if you used a film resistor, the high di/dt of the pulse is likely to cause a momentary breakdown between adjacent spirals). A good value for R2 would be 47 k or 100 k, also AB 1/2-watt carbon composition. Because this resistor is unlikely to see more than 300 V, it's not so critical, but I like to use carbon comp to remind me that film resistors aren't always preferable.

If you have a voltmeter with an $R_{in}$ of 10 MΩ, that's not quite as good as 1000 MΩ. But you will be able to see an indication that a 2-kV pulse does give something like a 200-mV jump. Heck, 180 is substantially the same as 200. But an indication of 160 or 130 mV would be wrong. This isn't necessarily a precision calibrator, but it's a pretty good lie detector. After all, it works on the conservation of charge (not the conservation of energy). The note we are putting on our ESD testers and calibrators says:

"1. Do not remove this calibrator under pain of death.
2. Many of these ESD testers have been known to fail in a mode with an actual pulse output amplitude of 1/2 to 1/4 of the indicated voltage.
3. Therefore, every day you use the tester, check its calibration. Set the pulse level to 2000 V and watch the output jump 200 mV for each pulse. If 4000 V, expect to see 400 mV. You can short the 1 µF to ground to reset it, or, just put your fingers across it.**
4. Calibration procedure is available from Cal Lab, Paragraph 93-14. (Measure total capacitance = 1.0 µF ±1% when R2 is shorted out.)"

# PEASE PORRIDGE

Anyhow, for the last 6 months I knew that I would eventually write a column on ESD, but I didn't have any strong motivation or impetus to do it. Nothing really important to say. But as soon as I recognized the importance of having a simple calibrator to help you catch your ESD tester as soon as it goofs up, that drove me to draft up and finish this column, pronto—and here you are.

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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** One of our legally oriented guys suggested a disclaimer: Whenever he hears the world "kilovolt," he doesn't want to go around touching anything, even if the DVM says 0.42 V... So, okay, go ahead and rig a push-button switch to short out the 1 µF, if you want to. BUT, a 4-kV pulse from a standard human-body-model tester doesn't BITE or TICKLE much at all. It sure doesn't hurt most people....

## BOB'S MAILBOX

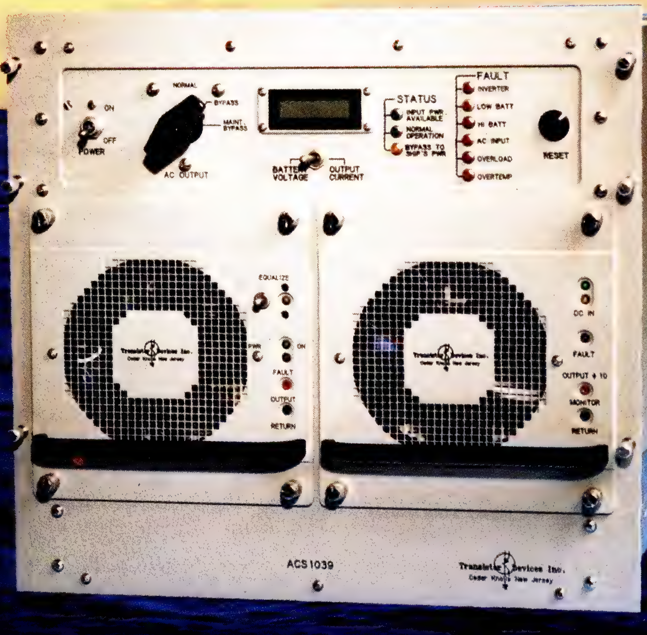
***Dear Bob:***

Regarding your notes on double-clutching in the August issue—as a veteran of driving our original family VW (a used 1951 model that my father acquired in 1953) I had to become expert at this, as the transmission was entirely non-synchro (presumably matching the mechanical brakes in mechanical simplicity). Upshifting (1-2, etc.) did not require double-clutching, but merely a short pause while the gears spin down to the appropriate speed for the next ratio.

...Of course, you did indeed have to double-clutch any time you needed to down-shift. The "blip" method was elegant and demonstrated considerable skill if executed properly. I had better luck, especially for shifts into first, if I released the clutch in neutral, accelerated the engine to the correct RPM for my speed (or slightly higher as you say), and then very quickly declutched and pulled it into gear. Easier to judge the RPM than a somewhat random blip of the throttle, and the engine speed would be correct for smooth engagement...

***PATRICK H. QUILTER***
***Costa Mesa, Calif.***

*Recently, my wet shoelaces flapping my leg twice every time I shifted, convinced me I really do double-clutch all the time. But I'm not sure I could handle a full-time crash-box. —RAP*



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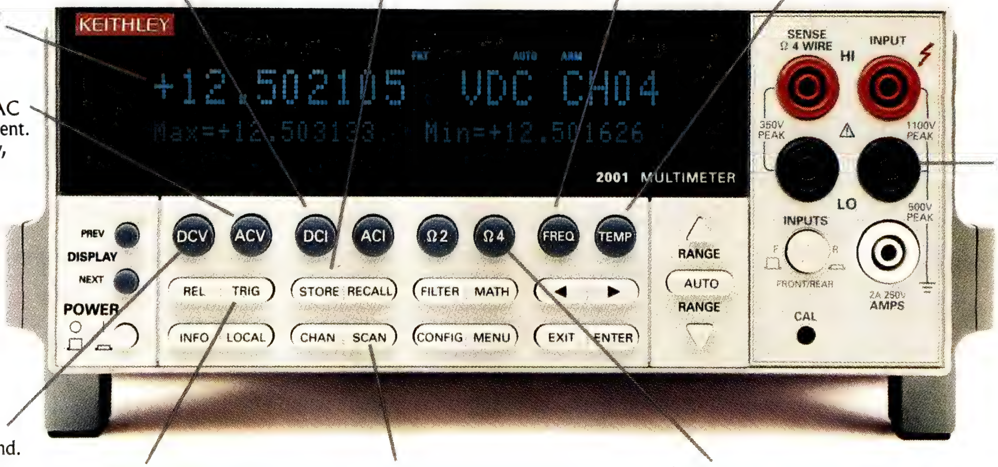

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UPDATE

# TEST & MEASUREMENT

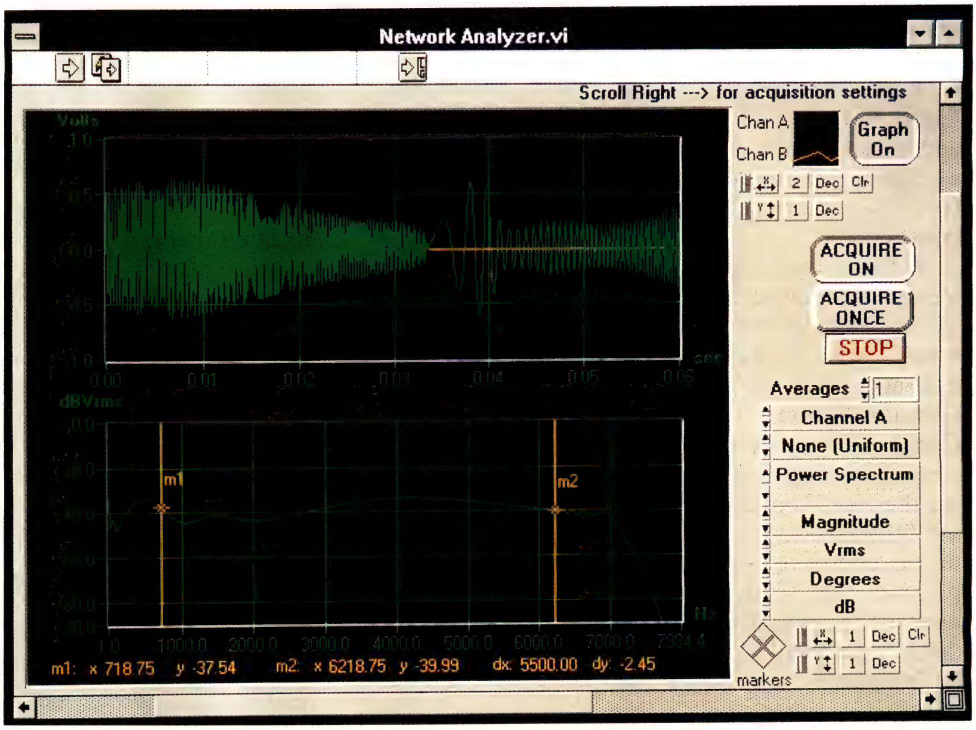
A SPECIAL EDITORIAL FEATURE

# Software paces data-acquisition advances

*Windows-based packages simplify programming of data-acquisition applications.*

BY JOHN NOVELLINO

Rapid-fire breakthroughs in data-acquisition technology, particularly in software, are placing more higher-performance, easier-to-use products at the disposal of systems designers. In addition to the continued improvement in speed and resolution that users of test and measurement equipment have come to expect, the introduction of several Windows-based software packages is simplifying data-acquisition programming. To top it off, competitive pressures are keeping prices from rising.



m1: x 718.75 y -37.54 m2: x 6218.75 y -39.99 dx: 5500.00 dy: -2.45

Many users have little or no programming experience, and they don't want to become programming experts. What they want is a hardware-software combination that lets them quickly get an application up and running with minimum hassle. The advent of Microsoft Windows allowed software vendors to offer an easy-to-use interface that's familiar to many engineers. An added benefit is the standardization that makes data exchanges easier.

As a result, software is often the "gating factor," the starting point for a designer specifying an entire data-acquisition system, according to Morris Samit, president of DSP Development Corp., Cambridge, Mass. Many designers presume, "Let me find the software I need, because once I find the software there's a lot of commodity hardware out there," says Samit. "The hardware manufacturers don't like to think of it that way. But the point is you select your software first. And then whether you buy a Sun Sparcstation or an HP 700 series or a DEC Alpha-based system is secondary."

Although Windows actually slows down data acquisition and analysis a bit, its advantages outweigh that negative. Users have been requesting Windows-based data-acquisition software for some time, and vendors have responded positively *(see p. 113).*

**Software is a major differentiating factor for purchasers of data-acquisition systems.**

Users often need more than one software package to perform the desired acquisition, display, and analysis functions. System designers have had to worry about the compatibility of these packages and whether data conversions should be made before users could exchange data between packages. Windows is changing that, however. "With hardware manufacturers having to write their internal software to be Windows compatible, the whole issue of interface drivers and exchanging data goes away," explains Samit.

The advantages to the user are obvious. "It's also a big boon to the manufacturers," says Samit. "We don't have to make sure that we can read data from this machine or that machine or accept data from some software package. We know we're going to be able to handle anything."

Another advantage of Windows is that it allows applications to be event-driven, rather than using a polling operation. This feature makes for more efficient programming and gives the programmer added flexibility in taking advantage of Windows' multitasking capability.

For example, say a user wants to collect 1000 sampled points in a polling system. The software would start the operation, then would poll the system after each point, asking the system whether the 1000th point had been collected yet. An event-driven system starts the operation, counts the points, and sends a message back when the last point is collected. In the polled system, the application is controlling the operation. In an event-driven system, the operating system retains control.

"I think you're going to be seeing more and more data-acquisition applications going that way," says Richard House, data-acquisition product manager for National Instruments Corp., Austin, Texas. "So instead of having a program that sits there and constantly polls to see if the data-acquisition operation is complete, you'll have a program that sends a message back to the application when it's done." As a result, Windows can be doing other tasks rather than constantly checking to see whether the data collection is completed.

To a large extent, data-acquisition hardware is becoming a commodity marketplace. Products are clustered around certain performance levels, such as 12- or 16-bit resolution and low-speed sampling rates for process control, or monitoring physical phenomena versus high-speed conversion aimed at electronic signals.

That leaves software as a major differentiating factor for data-acquisition systems. That's the route being taken by Data Translation, Marlboro, Mass., which sells both hardware and software. "You can differentiate your hardware a little bit," says John Hogan, general manager of Data Translation's data-acquisition group. "But it seems no longer possible to make it obvious why yours is superior."

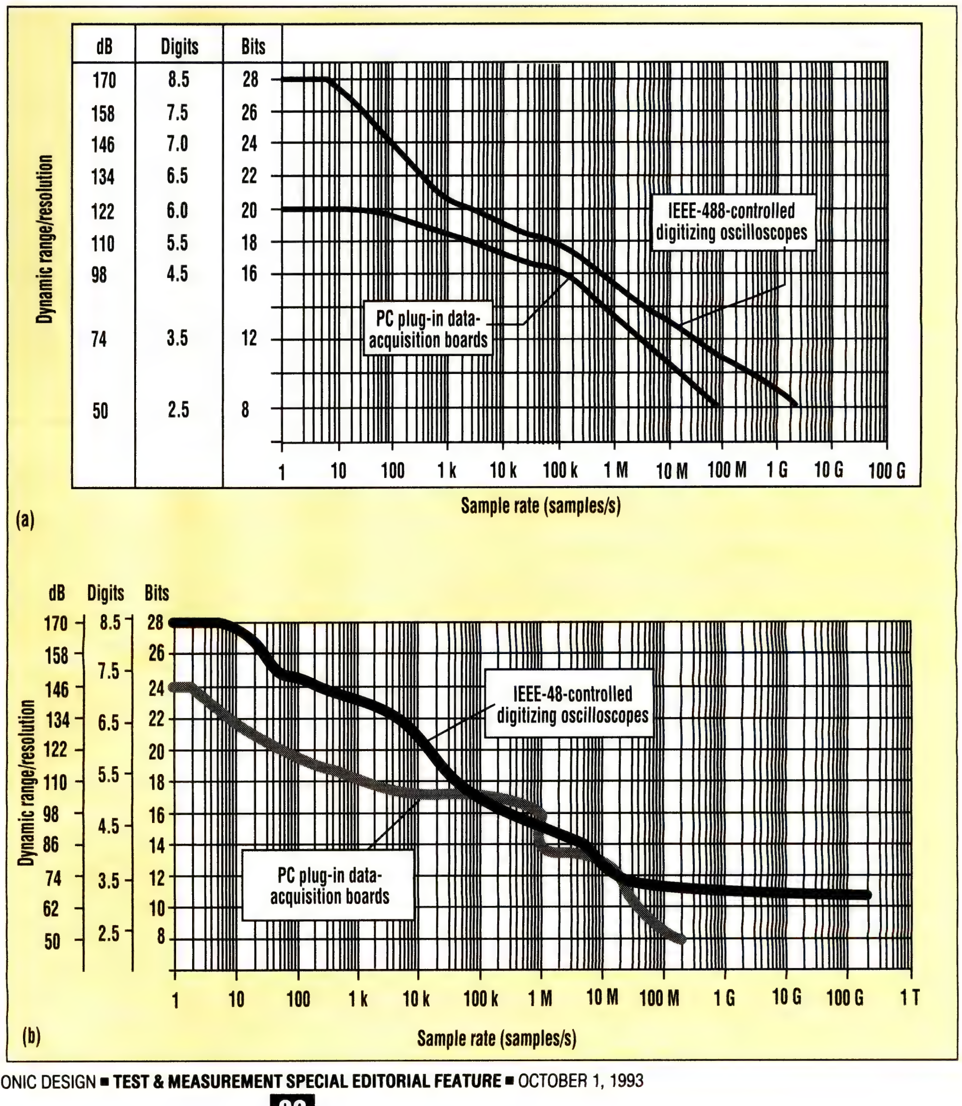
Hogan has seen an increased demand for very easy-to-use software. At the same time, more people are looking for vendors to provide over-the-phone technical support for both hardware and software. "As the business moves more to a commodity marketplace, I think those are going to be conflicting demands," he says. "I think you're going to see the face of the data-acquisition industry change. For example, people are probably going to have to start charging for technical support."

To remain competitive, data-acquisition vendors will have to work with end users, particularly large-volume customers, to help them come up with systems that meet their needs, according to Hogan. It may take a couple of years, but the large number of choices available will make this cooperation necessary. Technology changes, especially in sensors, also will be an important factor.

"I think that people who are going to survive in the data-acquisition business are going to have to do more joint development of systems with their larger customers," says Hogan.

Another important consideration for a large segment of data-acquisition users is portability. In the past, a portable system has usually meant a laptop computer containing expansion slots for plugging in data-acquisition boards. Their size and power

**With regard to key specifications, the gap between plug-in board performance and stand-alone instruments (represented by IEEE-488-controlled digitizing oscilloscopes) has narrowed considerably between 1990 (a) and today (b).**



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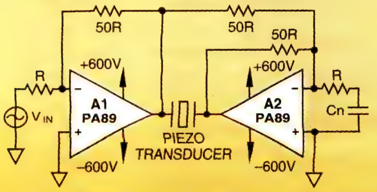

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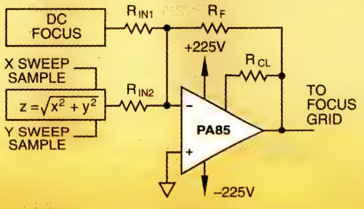

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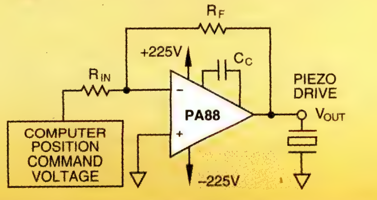

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consumption, however, created problems in many applications.

The solution is the notebook computer, according to Tom DeSantis, president of IOtech Corp., Cleveland, Ohio. Notebooks lack internal plug-in slots, so the data-acquisition peripherals must be external boxes that use the computer's serial or parallel ports. IOtech has moved into that arena with peripherals that mimic the notebook's form factor so they can be conveniently stacked beneath the computer in an integrated system.

Notebooks deliver the same performance as desktop IBM PC compatibles, and the smaller units' prices are starting to drop. The result is an excellent platform for data acquisition, says DeSantis. "They provide the user I/O, the computational capability, data storage, and communication," he continues. "They supply 90% of what our users of portable data acquisition need." The external boxes do the rest.

The proliferation of cloned plug-in boards has triggered a steep price erosion, according to DeSantis. He says users can get the same features today at half of what they paid a couple of years ago. "There's a strong drive towards reducing the cost of production," explains DeSantis. "It's more significant than in any other area of test and measurement."

National Instruments' House sees data acquisition beginning to encroach on the domain that used to belong exclusively to discrete instruments. One reason is the widespread use of personal computers, which means many potential users already have a key ingredient. With a PC-based data-acquisition system, the collected measurements go directly to the computer's memory, and are immediately available for processing and messaging. No transfers over a bus are required.

Another factor prompting the increased use of data acquisition is the improved performance of plug-in boards relative to standalone instruments. Figures collected by National Instruments show that over the last three years, the gap between the two alternatives has closed for a wide spectrum of frequencies. For sampling rates of about 100 ksamples/s to 20 Msamples/s, either data-acquisition boards or standalone instruments can do the job *(see the figure)*.

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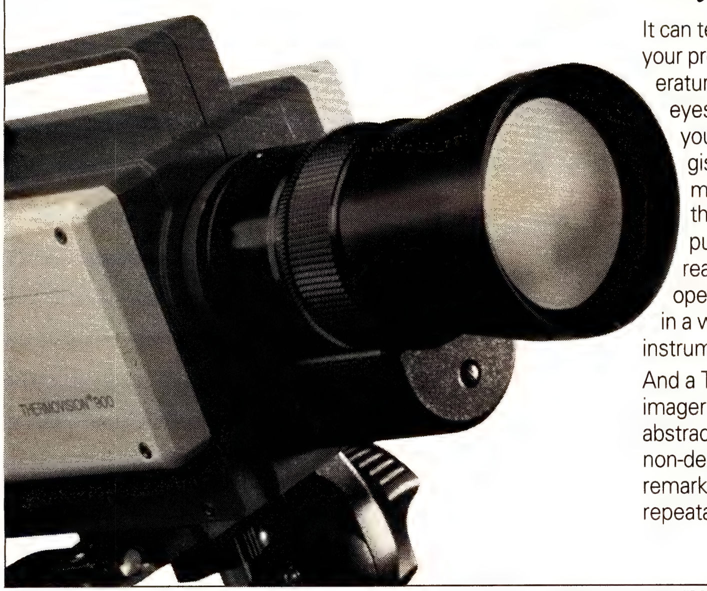

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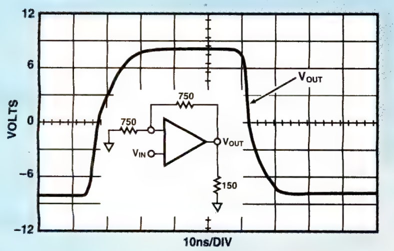

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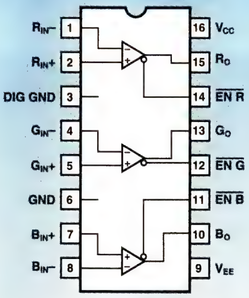

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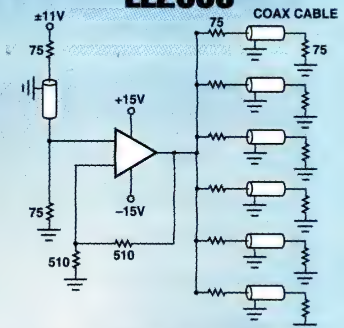

- Drives 6 – 150Ω Loads to ±11V
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- dG = .03%, dP = .05° @ NTSC/PAL
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## D.C. Restored Video Amplifier

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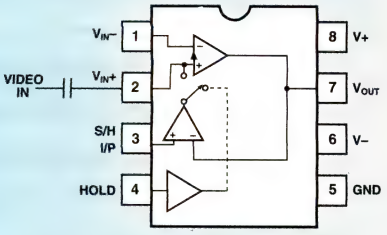

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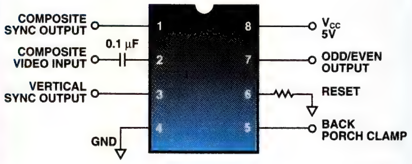

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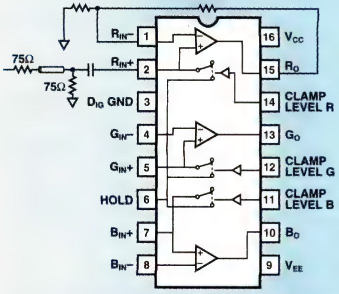
## EL4390



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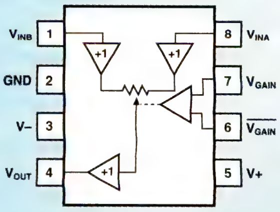

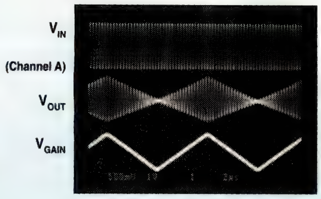

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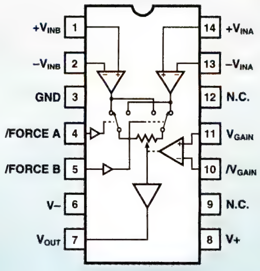

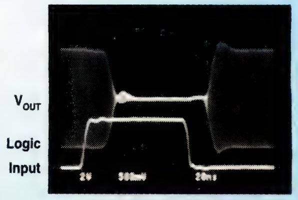

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# Data acquisition requires careful planning

*Designers must thoroughly define the system's tasks and functions before evaluating solutions.*

BY LESLIE LOGAN

Keithley Data Acquisition, 440 Myles Standish Blvd., Taunton, MA 02780; (508) 880-3000.

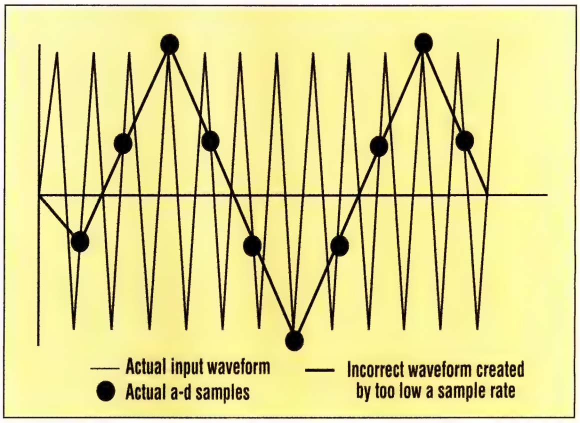
For many engineers, configuring a data-acquisition system is simply a means to an end, rather than the main focus of their responsibilities. For those with little or no experience in system integration, selecting appropriate hardware and software and combining them into a workable system that delivers usable information in a timely way can appear daunting. Fortunately, it doesn't have to be that way.

However, to avoid problems it's vital to take the time to define in advance what tasks and functions the system must perform. Those who begin buying hardware or software before completing this definition process are likely to spend far more money and time than necessary. Even worse, the system, once complete, may not live up to expectations.

Most modern data-acquisition systems employ a personal computer as a controller. A typical PC-based data-acquisition system consists of five basic elements: sensors or transducers that convert physical phenomena into a measurable signal; a computer platform; signal conditioners to isolate, convert and/or amplify the transducer signal; a data-acquisition subsystem; and data-acquisition software. Each must be considered in relation to the others.

In the most elementary sense, a data-acquisition system must perform three basic functions:

- convert the physical phenomena into a measurable signal,
- measure the signals produced by the sensors or transducers to extract information, and
- analyze the data and present the results in a useful form.



**1. If the acquisition system's sampling rate is too slow, the recorded results may indicate a waveform much slower than that of the actual signal.**

Therefore when selecting a sensor or transducer, the user must determine the magnitude of its signal, the smallest sensor output change that the system must be able to detect (the measurement resolution), and the speed at which the signal output must be measured.

As a rule, the computer platform for a data-acquisition system needn't be particularly powerful. However, when the application involves combining acquisition, analysis, and graphics, a more powerful computer, such as a 486-based unit, may well be worth the investment. Often the software selected will dictate the computer architecture required.

The most popular controllers for data-acquisition applications are the IBM PC/AT 386 and 486 compatibles, which use the Industry Standard Architecture (ISA) bus. The ISA bus performs 16-bit transfers at up to 500 kwords/s. Using a FIFO memory, special logic, and an IEEE-488.2 interface allows ISA transfers as fast as 1.5 Mwords/s.

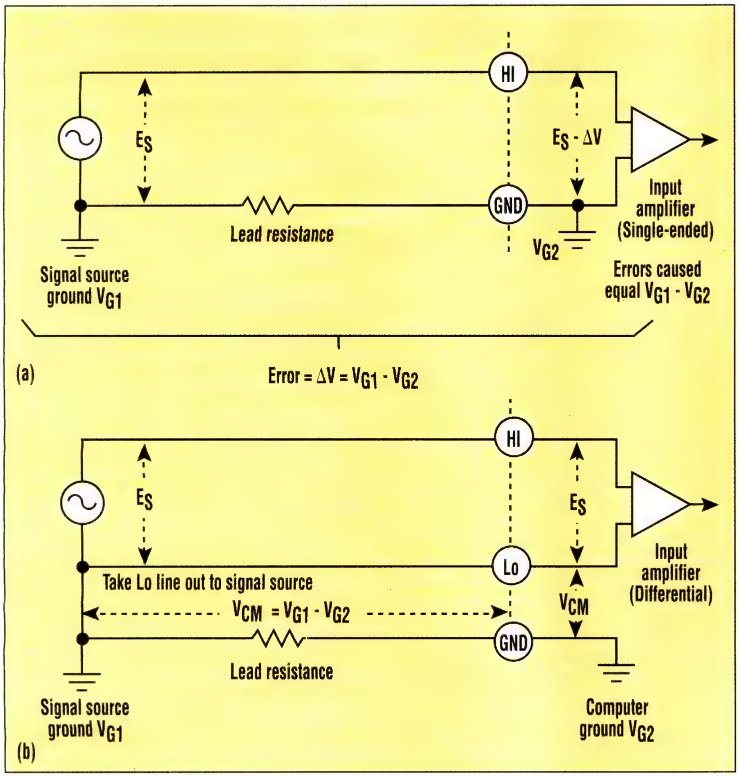
A growing number of data-acquisition products are also available for the Extended Industry Standard Architecture (EISA) bus, which is backward compatible with the ISA bus. The EISA bus extends the ISA address and data lines to 32 bits and adds extra control signals. The result is higher bus transfer rates and more direct memory access (DMA) channels and interrupt levels.

Finally, a number of products are available for the Apple Macintosh II NuBus, which is neither electrically nor physically compatible with the PC, PC/AT, or EISA bus. But like the EISA bus, the NuBus offers many higher-performance features that the PC/AT bus lacks. These include 32-bit data and address paths, high data transfer rates, bus arbitration, bus master capability, and automatic system setup.

Although each application will have unique requirements, several considerations will be common to virtually ev-

**TABLE 1: CONVERTER TRADEOFFS**

| Converter type | Speed | Resolution | Noise immunity | Cost |
|---|---|---|---|---|
| V/F counting | Slow | 16-24 bits | Very good | Medium |
| Integrating | Slow | 12-18 bits | Very good | Low |
| Successive approximation | Medium | 10-16 bits | Little | Low |
| Flash | Very fast | 4-10 bits | None | High |


HI
Es
Es - ΔV
GND
Input amplifier (Single-ended)
Lead resistance
$V_{G2}$
Signal source ground $V_{G1}$
Errors caused equal $V_{G1}$ - $V_{G2}$
(a)
Error = ΔV = $V_{G1}$ - $V_{G2}$
HI
Es
Es
Lo
Input amplifier (Differential)
Take Lo line out to signal source
$V_{CM}$ = $V_{G1}$ - $V_{G2}$
$V_{CM}$
GND
Lead resistance
Signal source ground $V_{G1}$
Computer ground $V_{G2}$
(b)

**2. Although a single-ended input (a) is simpler and less costly than a differential input (b), the differential input can offer significantly better noise immunity.**

ery system. In evaluating and selecting the components to fill them, keep in mind that if the hardware supports a particular function or capability but the software does not, the software might need modification or additional programming. The reverse is also true.

Most real-world signals are not well suited as direct analog-to-digital converter (ADC) inputs. Consequently, they usually need some form of signal conditioning—amplification, attenuation, or other modification—before an ADC can perform a useful conversion. Signal conditioning can occur in the data-acquisition subsystem or on an external board or module.

For the most accurate conversion, the input signal's full-scale deflection should match the ADC's input range. For example, if a sensor produces an output between ±1 V, then the full-scale input range of the analog input board should be ±1 V. Some data-acquisition hardware has a fixed input range, while other hardware has switch- or jumper-selectable input ranges. Still other hardware has software programmable ranges.

Fixed input hardware works well in systems with high-level inputs or where the signal conditioning is done by the sensor or instrument from which the data is acquired. Switch-selectable ranges are simple to understand and use, but can be unmanageable in systems that require frequent gain changes. Software programmable ranges can be used in any application, but typically cost more. Some systems also offer a choice between bipolar inputs (for example, ±5 V) and unipolar inputs (0-5 V).

**TABLE 2: PC-BASED VERSUS IEEE-488.2 INSTRUMENTS**

| PC-based Instruments | |
|---|---|
| Strengths | Limitations |
| Easy to program | Number of slots in PC |
| Portability | Performance |
| Price | Isolation |
| Space and size | |
| **IEEE-488.2 Instruments** | |
| Strengths | Limitations |
| High performance | Cabling |
| Wide range of instruments | More complex programming |
| Number of instruments in one system | Price |

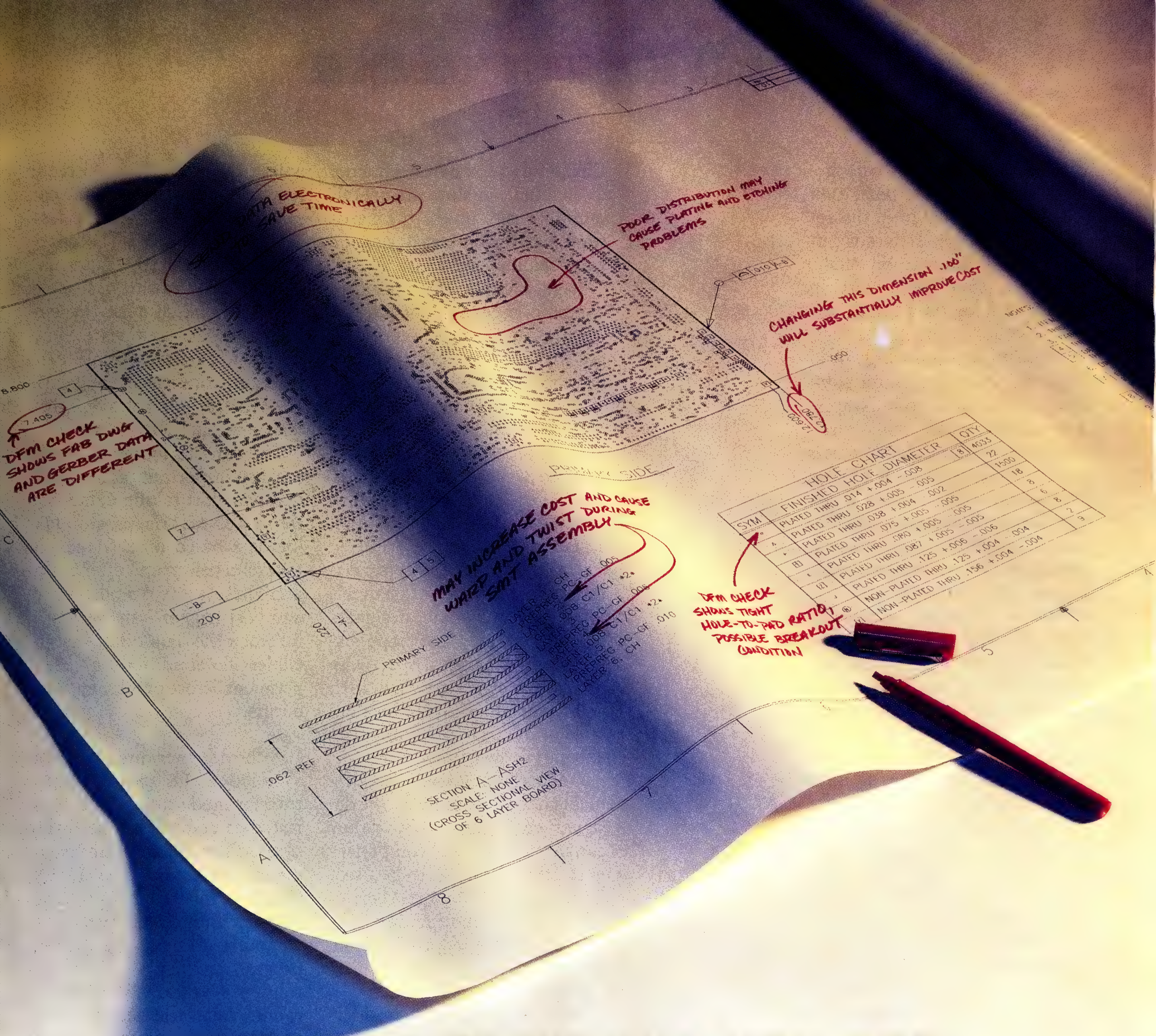
Many types of sensors need special conditioning circuitry. For example, thermocouples need cold-junction compensation, and RTDs and strain gauges require special excitation sources. The system must supply the proper inputs and outputs for these sensors.

Another form of signal conditioning is input isolation, which offers three main advantages. First, isolation protects the host computer from any high-voltage inputs that could damage the system. In addition, it protects the subject being tested from potentially dangerous voltages, such as after a failure in the computer or data-acquisition system. Thirdly, isolation can be a great way to eliminate ground loops. Systems with high gains or many different sensors or instruments can be plagued by excessive ground noise. Isolating the data-acquisition system's inputs from the noisy ground significantly increases measurement accuracy.

The engineer designing a data-acquisition system must consider several analog-input requirements, including resolution, input accuracy, maximum sampling rate, and number of channels.

*Input resolution.* This specification defines the smallest change in a signal that the system can detect. Resolution may be stated as a percentage of full-scale, but is more commonly expressed in bits. That is, a 12-bit system has $2^{12}$ possible output states so it can resolve to (measure) 1 part in 4096. Most data-acquisition products today deliver 12-bit resolution, but 8-, 10-, 14-, and 16-bit products are available. In general, higher-resolution ADCs are more expensive and slower than their lower-resolution counterparts.

*Input accuracy.* Accuracy is related to but not the same as input resolution. Accuracy is the maximum error of a measured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value with respect to its true theoretical value. Both resolution and accuracy must meet the application's needs. It is not uncommon to find a 16-bit ADC, which resolves to 1 part in 65,536, that has only 12-bit, or 1 part in 4096, accuracy.

*Maximum sampling rate.* Typically, the maximum sampling rate is specified in samples per second rather than hertz. Although sample theory states that a data-acquisition system must sample at least twice as fast as the highest frequency component in the input signal, most experienced system developers advise using a factor of three.

Too slow a sampling rate can cause aliasing. The system can incorrectly show a slow-moving signal that is actually a very high-frequency phenomenon *(Fig. 1)*. If signals to be measured contain frequencies above half the sampling rate, an anti-aliasing filter is recommended.

Most multichannel a-d products use one ADC and an input multiplexer. The multiplexer acts as a switch that allows each input channel to be sampled independently. Therefore, the maximum sample rate per channel is the maximum sampling rate of the ADC divided by the number of channels to be sampled. Often the maximum sampling rate is specified with all channels set to the same gain. Changing the gain from channel to channel can slow the overall sampling rate unless the hardware has an on-board gain or gain/channel queue.

High sample rates use up computer memory very quickly. As a result, the length of time a system can sample data is just as important as its sampling speed. To ensure sufficient sampling time, the controller may need additional RAM or the user may have to write or acquire high-speed disk-access software (sometimes called a "disk streamer").

*Number of channels.* Although the number of channels may seem obvious, designers should consider that applications tend to expand. Specifying hardware and software with greater channel capability than current needs often simplifies expanding the system later.

Once these system requirements have been defined, the designer can examine how they can be met. One key component is the type of ADC to be used. There are four common types of ADCs: V/F counting, integrating, successive approximation, and flash. Each has its own performance tradeoffs *(Table 1)*.

Another important consideration is a-d triggering. Particularly in applications such as frequency and FFT analysis, any jitter in the intersample timing will cause large errors. Also, the loss or skipping of a sample can easily render the data useless. The a-d conversion should be initiated directly by the pacing clock in the hardware or from an external clock. Systems that employ software routines to start conversion are susceptible to jitter. Hardware triggers and gates allow better control over when data is taken, saving memory.

The sample modes available are also important. Some products can start taking data when they receive a trigger, stop taking data based on a trigger, or take data before and after a trigger. These last two modes—pre- and post-trigger—are very useful when the data of interest includes the condition of the experiment before or after an event occurs.

The designer must also consider the type of data-transfer mode to be used. Most fast data-acquisition hardware uses either interrupt-driven or direct memory access (DMA) transfers. In an interrupt-driven transfer, an interrupt causes the computer to halt the current program and jump to a different routine. Typically, the second routine takes the data from the acquisition hardware, puts it into memory, and performs any other desired tasks before returning control of the computer

## PITFALLS TO AVOID

Although each system has its unique problems, there are a few common pitfalls that developers should be aware of before making a hardware or software purchase:

*Pitfall No. 1.* Trying to select hardware or software without a clear understanding in advance of the capabilities it must provide. The "I'll-figure-it-out-as-I-go-along" approach is a sure prescription for failure.

*Pitfall No. 2.* Choosing a software vendor that does not offer a run-time or site license. This is important if it is likely that more than one person will need to use the application or if it will be expanded.

*Pitfall No. 3.* Allowing "too many cooks to spoil the broth" when getting a consensus for purchasing hardware or software. Some companies assign separate hardware and software "gurus" to a project, and often neither speaks the other's language. This confusion makes it nearly impossible for vendors to support the system properly because it's difficult to get a concise description of the problem. The hardware expert has no idea how the program works, while the software expert doesn't understand anything about the connections or incoming signals. There should be a manager who understands the overall system and who will make the final decision about which hardware and software to buy.

*Pitfall No. 4.* Prematurely eliminating hardware or software that doesn't include every capability everyone involved might possibly ever need or want. Don't shut out options that are otherwise very well-suited to the application. Keep expectations reasonable.

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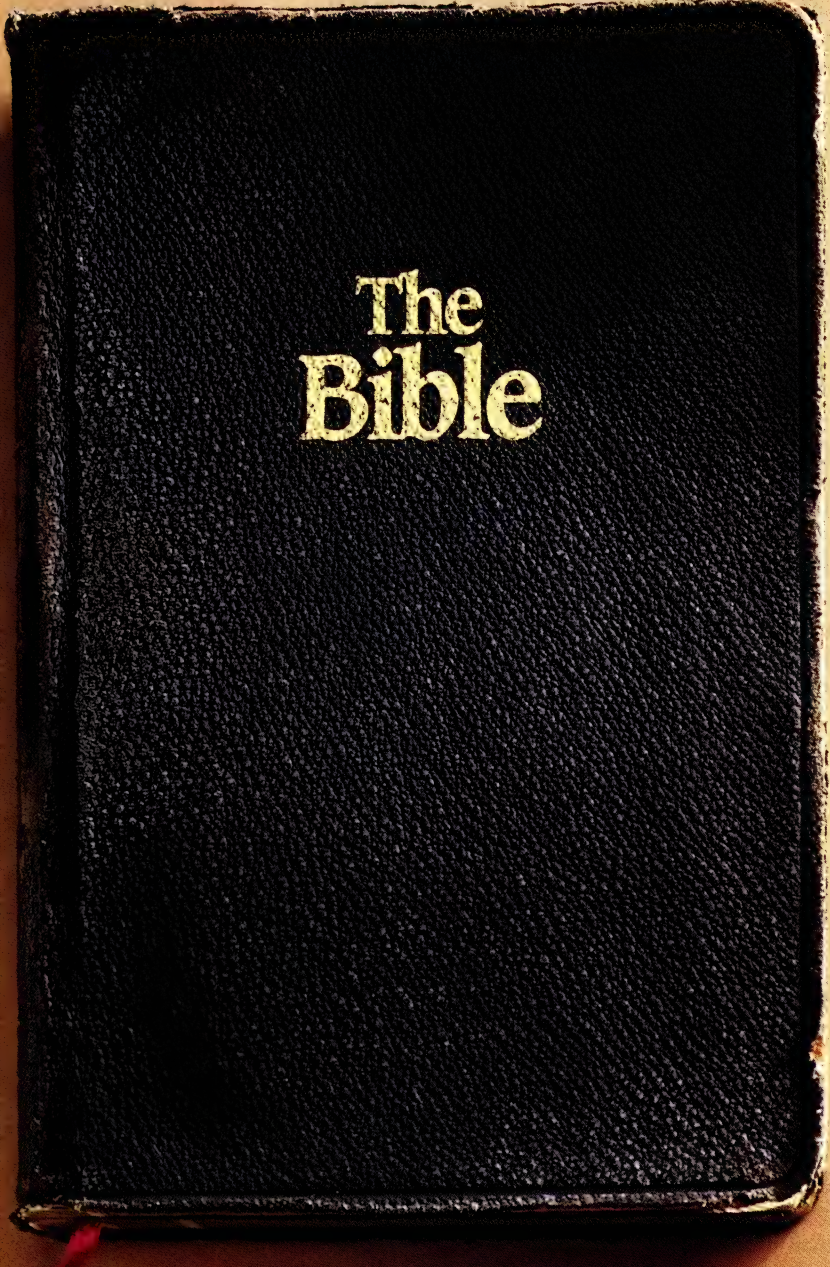

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to the original program.

On the other hand, a DMA transfer takes the data from the acquisition hardware and puts it directly into the computer's memory. After transferring 64 kbytes of data (typically 32-k data points) the DMA controller has to be reprogrammed. To avoid losing data, an on-board FIFO buffer can be used to store data during the reprogramming. Alternatively, a second DMA channel can be added so one channel can be transferring data while the other is being reprogrammed.

Because DMA transfers are completely hardware controlled and are performed in the background, they are extremely fast. But in lower-speed applications interrupt-driven transfers may be adequate. A number of extremely fast products employ on-board memory, so they are not limited by the computer's bus speed.

The final choice in the a-d subsystem is between single-ended or differential inputs *(Fig. 2)*. Although differential inputs are somewhat more complex to use and more expensive than single-ended configurations, a differential input usually offers better noise immunity. The differential input reduces the error caused by the common-mode voltage, $V_{CM}$, by the amount of common-mode rejection of the input amplifier, which is typically 80 dB or greater. This is especially important in systems that take data from a number of different devices or in systems that are located far away from the actual input sensor or instruments.

Besides the a-d function, most data-acquisition systems also use some combination of analog outputs, digital inputs and outputs, counter-timers, motor controllers, and other functions. These features are needed if the system must not only acquire data but also control a test or process.

The most often used of these functions is digital I/O lines. Digital inputs *monitor* switch closures, sense power on-off conditions, and read data from a wide varaiety of devices with parallel digital outputs. Digital outputs can turn power on or off, control motors and heaters, activate relays, and write data to devices with parallel digital inputs. Digital interfaces are also available for continuous high-speed communications.

Analog outputs generate excitation voltages and waveforms, control valves, and simulate outputs from other devices. Specifications for analog outputs are expressed in much the same terms as for analog inputs.

Counter and timing functions are often needed to set sample rates accurately on analog inputs and outputs. They are also useful for measuring frequency, counting events, measuring time and delays, and generating output frequencies.

Acquired data is of little value if the system can't display and analyze it. So the system designer must evaluate how sophisticated the display and analysis capabilities must be, taking into account the intended user.

Finally, a study of system requirements should include future growth. Most applications evolve or expand over time, so it's wise to allow some capacity for additional channels, faster acquisition speeds, and such without the need to buy new hardware or software.

Once these basic requirements have been set, users can evaluate the available options. To define a total solution, it's important to examine hardware and software options simultaneously, rather than choose the hardware first, then search for compatible software or vice versa.

Two of the most common types of hardware alternatives are plug-in multifunction data-acquisition boards and external chassis systems with multiple single-function boards. While the two approaches overlap somewhat, designers can generally select the more appropriate configuration through a careful analysis of their application's current and future needs.

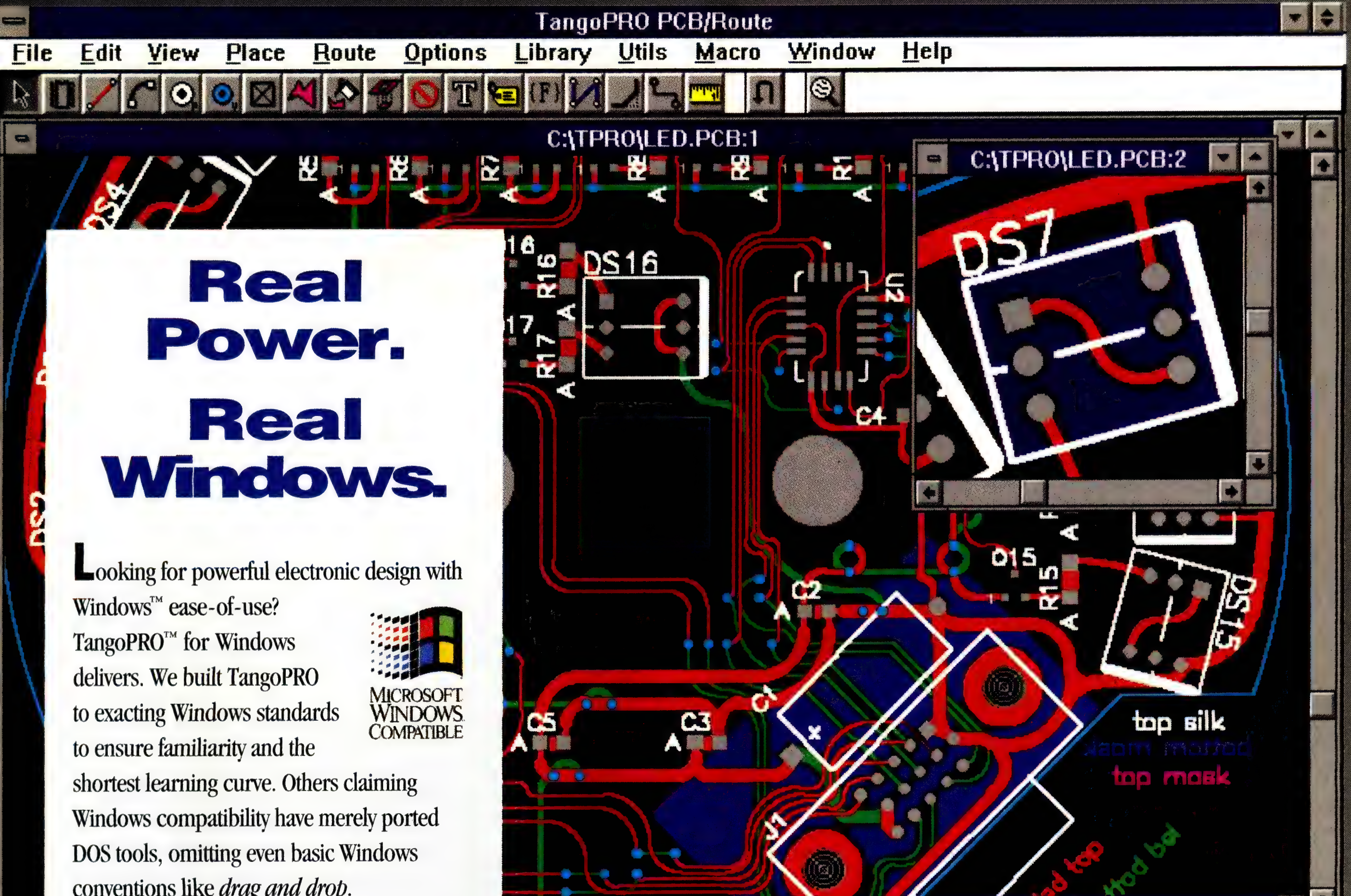
**Programming a data-acquisition system in a high-level language offers the greatest flexibility for customization.**

A plug-in, general-purpose, multifunction board plugs directly into a PC's expansion slot. A connector that extends outside the computer links the board to the signal inputs and outputs of the sensors or transducers being monitored or controlled. These boards offer a number of advantages.

First, because the board uses the PC's power supply and enclosure, these applications often cost significantly less than solutions that need a separate enclosure and power supply. While typical plug-in board prices range from $200 to $3000, depending upon their capabilities, systems based on multiple single-purpose boards housed in an external chassis start at around $1500 and can cost $5000 or more. If bench or rack space is at a premium, multifunction boards require no more room than the PC itself. And since they plug directly into the PC's bus, the boards transfer data directly into the computer's memory at full bus speed.

As the name implies, general-purpose multifunction plug-in boards supply several functions: analog input, analog output, digital I/O, counter-timer, etc. They are well-suited for applications with relatively low channel counts (generally less than 32) and high sample rates for tracking rapidly changing phenomena like voltage levels. However, by using an expansion chassis and interface, a designer can extend the PC's capacity by up to 12 additional slots.

Also, a variety of analog expansion boards and external signal-conditioning hardware are available to increase the number of input channels being monitored by a data-acquisition board, condition the input signal prior to measurement by the board, or provide electrical isolation for the system. But these interfaces must be physically



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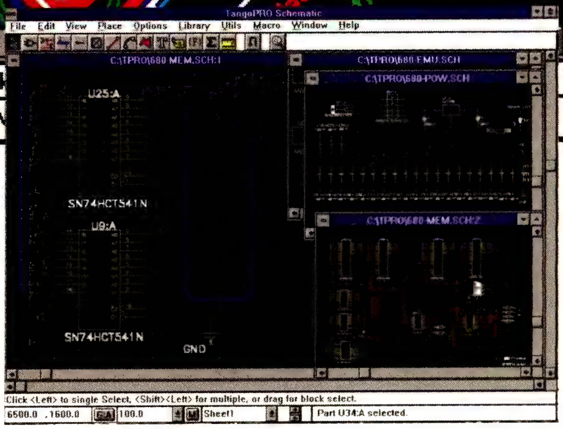

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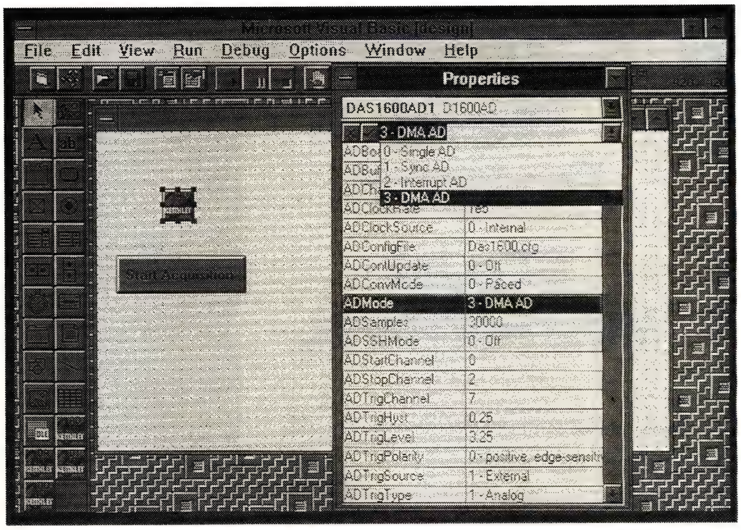
Another advantage of plug-in, multifunction boards is the broad range of software available to aid in applications development. Designers may want only a board driver to use as the basis for creating an application with a high-level programming language like C, Basic, or Pascal. Or they may want a complete, integrated development platform. Either way, they're likely to find a compatible software product.

Because of their relatively low cost, flexibility, and high speed, general-purpose multifunction boards are very popular for a wide range of laboratory automation tasks, like monitoring and controlling experiments. They are also often used in engineering test applications, like developing or characterizing new devices, components, or processes, and in production testing of products such as computer disk drives.

Note that these applications typically demand a relatively low channel count. Size constraints limit the number of functions and channels that can be built on one board. Reasonably high data-acquisition rates are common, but the computer's noisy environment can degrade signal integrity.



DAS1600AD1 D1600AD

| | |
|---|---|
| ADClockSource | 0 - Internal |
| ADConfigFile | Das1600.cfg |
| ADContUpdate | 0 - Off |
| ADConvMode | 0 - Paced |
| ADMode | 3 - DMA AD |
| ADSamples | 30000 |
| ADSSHMode | 0 - Off |
| ADStartChannel | 0 |
| ADStopChannel | 2 |
| ADTrigChannel | 7 |
| ADTrigHyst | 0.25 |
| ADTrigLevel | 3.25 |
| ADTrigPolarity | 0 - positive, edge-sensiti |
| ADTrigSource | 1 - External |
| ADTrigType | 1 - Analog |

**3. Using custom controls for Visual Basic simplifies data-acquisition programming for Windows. Buttons or control panels let users focus on data-acquisition applications, instead of programming details.**

Single-function boards are often designed to be housed in an external chassis, rack, frame, or NEMA enclosure. Communication with the single-function board is through a cable connected to an interface board plugged into the host PC. Single-function boards typically have a much higher capacity for performing their lone functions than a multifunction board does. For example, while a typical multifunction board might have one or two on-board counter-timers, a single-function counter-timer board could have eight or more. If the application expands later, the system can usually be modified fairly simply by installing another board in the enclosure.

Applications for single-function boards generally have relatively low sampling rates and high channel counts. The parameters being measured are usually relatively slow to change, like contact closures, temperatures, pressures, etc.

Single-function boards are well-suited to applications that need signal conditioning with isolation. While electrical isolation is usually less critical in scientific applications, it may be important in the electrically harsh industrial environments in which single-function boards are often used. Opto-couplers or transformers supply this high level of isolation.

Single-function boards in industrial environments are part of the continuing trend away from centralized data-acquisition and analysis systems and toward an architecture that distributes intelligence more evenly throughout the system. Increasingly, single-function boards are used in conjunction with a dedicated controller located in the same framework. The dedicated controller and boards are responsible for handling lower-level tasks, such as data acquisition and reduction, simple monitoring, and control.

Under a highly centralized system with a single computer, these tasks often slowed system reaction time to a virtual standstill. Off-loading these responsibilities onto the dedicated controller and single-function boards frees larger, central controllers to handle supervisory and analytical functions more efficiently.

The software for systems built of single-purpose boards is usually developed with industrial applications in mind. Supervisory and control functions for process monitoring and regulation tasks are generally included. Compared with the wide range of options available to scientific and engineering users of multifunction boards, there are significantly fewer "flavors" of packaged software from which the industrial user of single-function boards may choose.

Because of their high channel counts and easy expandability, single-function boards are commonly employed in machine control or process monitoring and control systems. They are also popular for supervisory control and data-acquisition applications like environmental control, alarm monitoring, and temperature and level control, in which measurements are reported to a central station via modem or RS-422 serial link.

"Feature creep" is common. As a system is developed, it's easy to give in to the desire to keep adding capabilities. This tendency can quickly increase

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the system's channel count far beyond that originally envisioned. If this seems likely, remember that it's usually far easier and possibly less expensive to expand a system based on single-function boards than to expand one based on a general-purpose multifunction board.

Several other hardware approaches may be appropriate for some applications. For example, many benchtop instruments can be programmed via the IEEE-488.2 bus. A wide variety of these instruments, which can be controlled from any computer with an IEEE-488.2 interface board, are available for data-acquisition applications. Such instruments generally have higher performance and more features than plug-in boards.

In recent years, a number of lower-cost alternatives to traditional programmable instruments have been developed. These units, which reside on a PC plug-in board, and their accompanying device driver software allow users to configure a test system easily. Many of these instruments have a software-generated front panel that can be displayed on the PC's screen. A keyboard or mouse controls these "virtual instruments" in the local mode. Most can also be programmed much like an IEEE-488.2 instrument in the remote mode.

Board-level instruments commonly include many of the features found in conventional instruments, including timing or state displays, data logging, menu-driven programming, autoranging, trigger options, and short-circuit and overload isolation. Their performance is roughly equivalent to many low-end IEEE-488.2 units. However, the space and noise limitations within a PC make truly high-performance boards impractical *(Table 2)*.

Additional benefits of PC-based instruments include the ability to control all instruments from one interface, easy communication over the computer bus rather than external cabling, and easy portability for remote applications and field testing. Also the cost of PC-based instruments is often significantly lower than that of a similarly specified IEEE-488.2 unit. The PC-based version contains only the measurement section and the simple PC bus interface, with the computer providing other needed functions.

Software can be the most expensive part of a data-acquisition project, after the cost of development, testing, and maintenance are added to the purchase price. As noted, the hardware and software for a data-acquisiton system should be evaluated simultaneously. The system integrator must make certain the software can support all the functions required of the hardware, and vice versa. Choosing either component before beginning to evaluate the other can lengthen the selection process. Suppliers are constantly revising and improving their products, so it's best to buy the hardware and software at roughly the same time to prevent them from being "out of sync."

The software spectrum ranges from the "do-it-yourself" programming approach (using drivers and any number of high-level programming languages) all the way up to powerful, yet easy-to-use application development packages. Before committing to any software development approach, the system integrator should understand the tradeoffs involved. Typically, these include ease of use versus power, price versus functionality, and solutions to immediate needs versus the flexibility to grow as needs change.

Programming a data-acquisition system in a high-level language like C, Pascal, or Visual Basic takes longer than using an application development package, but it offers the greatest flexibility for customization. Specialized programming environments have also been developed for creating engineering and scientific applications. These products are best suited for experienced developers or for those with highly specialized applications that demand maximum flexibility.

**Because DMA transfers are completely hardware controlled and are performed in the background, they are very fast.**

Fortunately, numerous readily available tools simplify the programming of a custom application. Examples include utility programs that generate control code for IEEE-488.2 instruments. And the graphical environment of Windows 3.X makes it a natural partner of a data-acquisition board when a designer must create custom control panels and user interfaces. Many board suppliers now provide software drivers to support languages that run within Windows 3.X.

Some hardware manufacturers produce Windows-based drivers packaged as dynamic link libraries. These drivers operate just like any DOS-based driver, except that they work within the Windows operating system. The user writes a short program that calls the driver, and the driver handles all the communication with the board.

Data-acquisition programming in Windows has become even easier with the advent of custom controls for Visual Basic, which are available from several vendors. A user simply installs the data-acquisition custom control into the Visual Basic toolbox, and when a control is activated, a property list for a particular function is displayed. The user then fills in information like acquisition mode, clock rate, and the channels to be scanned. Buttons or control panels can be added to initiate data acquisition. The custom control shields users from the complexity of the driver, allowing them to focus on the application, rather than on programming details *(Fig. 3)*.

At the other end of the spectrum are integrated software packages, which offer off-the-shelf, ready-to-use capabilities to get an application started fast. These packages are popular with users who haven't the time, background, or desire to do their own programming.

Integrated packages handle most facets of an application, allowing the user to acquire data, control instruments or plug-in boards, and display and analyze results within the same environment. Some packages can automate repetitive tasks or set up custom menus and virtual front panels to make the application easier for other operators to use. As a rule, however, the easier a package is to use, the less flexibility and adapability it supplies.

While evaluating software development approaches, it's also a good idea to make a frank evaluation of the resources available. Questions to ask include:

- •Can the application developer modify or expand software or does he or she have access to someone who can?
- •Will the project's budget accommodate extensive software modifications?
- •Does the time frame permit sufficient development and modification time?

Another consideration is the ease-of-use required of the finished application. The developer must know who will be using the system. If inexperienced users will run the system, its operation must be obvious and intuitive. A menu- or icon-driven interface will help guide the selections and simplify operation. A custom control panel—one created with specific users in mind—can be the easiest interface of all.

A growing number of integrated software packages include tools that let virtually anyone create a sophisticated, yet easy-to-understand, user interface. While it's certainly possible to create such interfaces through programming, the added work involved can make developing them impractical.

Choosing a software approach doesn't have to be an either-or proposition. Many applications can benefit from combining elements of an integrated package with a programming language. For example, an integrated package can support programming work. The package can verify setups, document responses, and test algorithm flows. Conversely, conventional programming can extend the package's capabilities. Many packages will accept custom routines written in C.

When evaluating hardware and software, it's easy to become overwhelmed by all the options available. To narrow the list, double-check that the software supports all required hardware capabilities (and vice versa) or can be created within an acceptable timeframe and budget. Whenever practical, obtain loaner packages, demo disks, and loaner hardware. "Test drive" each, both separately and in combination, before committing to a purchase that might not be appropriate.

Although the number of data-acquisition hardware-software combinations grows by the day, many sources of information are available to guide the new system developer through the selection and integration process. Don't be afraid to ask for help. Product literature, demo disks, loaner units, recommendations from colleagues or users of a particular piece of hardware or software, and independent evaluations, are all good ways to gather data. Hardware and software suppliers can also help in analyzing applications requirements and can often provide guidance in finding solutions.

*Leslie Logan is the product marketing manager for data-acquisition boards at Keithley's Data Acquisition Div. She received her BSEE and MBA from Cornell University, Ithaca, N.Y.*

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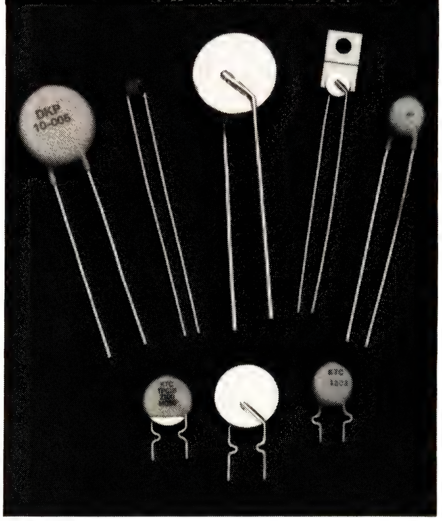

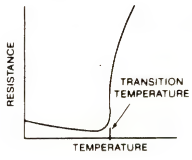

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(714) 859-8999
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Seattle, WA 98107
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Solon, OH 44139
(216) 349-4030
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**Second Wave Inc.**
9430 Research Blvd.
Echelon II, Suite 260
Austin, TX 78759
(512) 343-9661
**EMD, MPB**
**CIRCLE 701**

**Sheldon Instruments**
1021 N. University Ave.
Suite 204
Provo, UT 84604
(801) 377-2525
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**CIRCLE 702**

**Signalogic Inc.**
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No. 111
Dallas, TX 75243
(214) 343-0069
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**Signatec Inc.**
357 N. Sheriden St.
Suite 119
Corona, CA 91720
(909) 734-3001
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Sunnyvale, CA 94086
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**Tektronix Inc.**
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P.O. Box 500
MS 39-710
Beaverton, OR 97077
(503) 627-4602
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**Virginia Panel Corp.**
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Waynesboro, VA 22980
(703) 949-8376
**VXI**
**CIRCLE 708**

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N. Attleboro, MA 02760
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(508) 695-8459
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**Wavetek Corp.**
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San Diego, CA 92123
(619) 279-2200
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**CIRCLE 710**

**Yokogawa Corporation of America**
2 Dart Rd.
Newnan, GA 30265
(404) 253-7000
**AH, AI, INC, PAA, RTA**
**CIRCLE 711**

### KEY

**Hardware**

| | |
|---|---|
| **(AH)** | Analysis hardware |
| **(AI)** | Analog input |
| **(AO)** | Analog output |
| **(DIO)** | Digital I/O |
| **(EMD)** | External Macintosh devices |
| **(EPD)** | External PC devices |
| **(FA)** | Fixtures and adapters |
| **(II)** | IEEE-488 interfaces |
| **(MPB)** | Macintosh plug-in boards |
| **(PPB)** | PC plug-in boards |
| **(SAS)** | Stand-alone systems |
| **(SC)** | Signal conditioning |
| **(VXI)** | VXIbus |

**Software**

| | |
|---|---|
| **(DD)** | DOS drivers |
| **(ICO)** | Icon-based |
| **(INC)** | Instrument control |
| **(MD)** | Macintosh drivers |
| **(MEN)** | Menu-based |
| **(PAA)** | Post-acquisition analysis |
| **(PAG)** | Post-acquisition graphics |
| **(RTA)** | Real-time analysis |
| **(RTG)** | Real-time graphics |
| **(WD)** | Windows drivers |

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CIRCLE 209 FOR RESPONSE OUTSIDE THE U.S.

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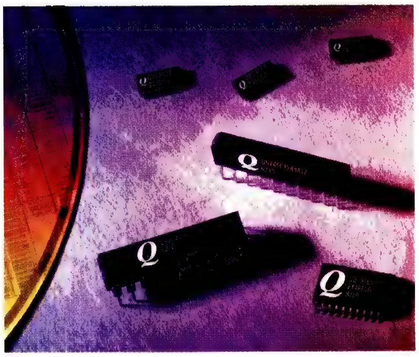

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**Quality Semiconductor, Inc.**
851 Martin Avenue, Santa Clara,
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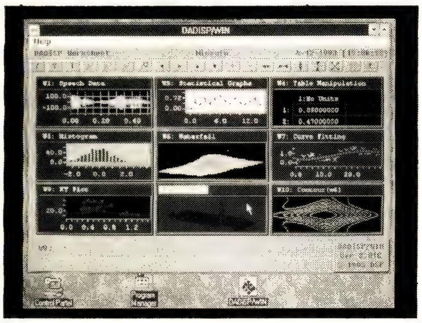
CIRCLE 210 FOR U.S. RESPONSE CIRCLE 211 FOR RESPONSE OUTSIDE THE U.S.

## ▼ GRAPHICAL ANALYSIS SOFTWARE GOES WINDOWS

DADiSP/32-WIn is a 32-bit native Windows version of DADiSP, the graphical data analysis software. The new package is 100% compatible with previous releases, so existing worksheets, data sets, macros, and command files will operate without change. As a native Windows application, the software can run multiple applications, import data via the Notepad utility, perform clipboard cut and paste, and manage memory allocation, among other things. Some of the new features included are icon buttons for sessions control and data manipulation, Sobel edge detection, and time and data stamping. DADiSP/32-WIN costs $995. Current DADiSP users under maintenance can buy the new version for $495. For those not under maintenance, the price is $795.



***DSP Development Corp.***
*1 Kendall Sq.*
*Cambridge, MA 02139*
*(617) 577-1133*
**▶ CIRCLE 719**

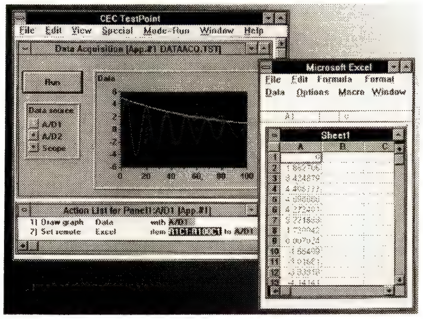
## ▼ SOFTWARE MAKES USE OF WINDOWS MULTITASKING

The Windaq/200 multitasking data-acquisition software allows users to acquire and record waveform data to disk in the background while operating other Windows applications in the foreground. Used with the previously released Windaq Playback and Analysis packages, users can acquire, review, store, and analyze waveforms without leaving the Windows programming environment. The software can handle up to 16 channels at once at speeds to 83,000 samples/s. Windaq/200 is compatible with four high-speed, digital-signal-processor-based boards introduced last year. Real-time display capabilities include smooth scrolling, freeze, autosweep, or triggered sweep. More than 8000 events per file can be time- and date-stamped. Windaq/200 is priced at $595.

***Dataq Instruments Inc.***
*150 Springside Dr.*
*Suite B220*
*Akron, OH 44333*
*(216) 668-1444*
**▶ CIRCLE 720**

## ▼ WINDOWS ICONS SIMPLIFY TEST PROGRAMMING TASK

A data-acquisition, analysis and presentation software package called TestPoint allows designers to build test procedures on screen by selecting Windows icons for input, output, display, control graphics, and calculations. All icons are highly intuitive and designed to match the "look and feel" of standard test concepts, definitions, equipment, and procedures. The designer first chooses which devices and functions are needed for each test (objects), and then lists the proper sequence of steps, measurements, and procedures (actions). The icons are dragged and dropped into a display panel or action list. The software, which runs on 80286-based or higher PC compatibles, can control IEEE-488 or RS-232 instruments, or data acquisition boards. TestPoint costs $995.


CEC TestPoint
File Edit View Special Mode-Run Window Help
Data Acquisition [App.#1] DATAACQ.TST
Run
Data source
A/D1
A/D2
Scope
Data
Action List for Panel1:A/D1 [App.#1]
1) Draw graph Data with A/D1
2) Set remote Excel item R1C1:R100C1 to A/D1
Microsoft Excel
File Edit Formula Format
Data Options Macro Window
Sheet1

***Capital Equipment Corp.***
*76 Blanchard Rd.*
*Burlington, MA 01803*
*(617) 273-1818*
**▶ CIRCLE 721**

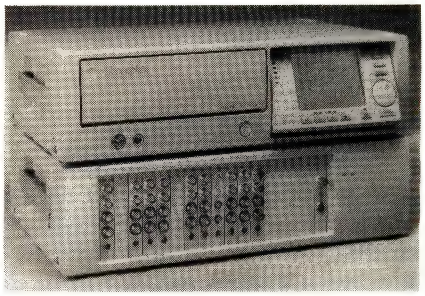
## ▼ PC-BASED DATA SOFTWARE WORKS IN WINDOWS

A data-acquisition, analysis, and display software package, Signalyzer, supports the Intelligent Instrumentation line of PC-based data acquisition boards in the Windows environment. The software captures up to 32 channels of data with sample rates to 10 MHz. Data can be acquired in bursts to PC RAM or streamed continuously to disk. Analysis capabilities include time- and frequency-based functions with or without a math coprocessor. The software includes real-time oscilloscope and signal analyzer displays. Optional Digital Filter Design software adds FIR and IIR filter structures for low-pass, high-pass, bandpass, and notch filters. Signalyzer (part number PCI-20395S-1) is available off-the-shelf for $495. The Digital Filter Design package (PCI-20396S-1) costs $295.

***Intelligent Instrumentation***
*6550 S. Bay Colony Dr.*
*MS 130*
*Tucson, AZ 85706*
*(602) 573-0887*
**▶ CIRCLE 722**

## ▼ DATA RECORDER HANDLES 64 CHANNELS REMOTELY

Designed for either laboratory or field use, the Storeplex portable instrumentation recorder offers remote control operation in a modular architecture. The unit has a 64-channel capacity, 96-dB dynamic range, 16-bit analog-to-digital conversion, and a 68-Gbit data storage capacity using enhanced super-VHS helical-scan technology. Users can mix analog (up to 45.5 kHz) and digital (up to 12.8 Mbits/s) channels. The tape transport unit holds the S-VHS tape transport and all read/write primary formatting and electronics for 64 channels. The signal processing unit contains input-output interfacing, sampling, multiplexing, and secondary formatting for 32 channels. An optional signal extension unit offers an additional 32 channels. The remote control unit includes the control and display functions. Storeplex recorder prices start at $34,000.



***Racal Recorders Inc.***
*15375 Barranca Pkwy.*
*Suite H-101*
*Irvine, CA 92718*
*(714) 727-3444*
**▶ CIRCLE 723**

### ▼ PORTABLE DATA SYSTEM HAS SELECTABLE SAMPLING

The Megadac 3108AC portable data-acquisition system delivers selectable sample rates up to 25,000 samples/s and 16-bit dynamic range with 1 μV sensitivity. The system features intelligent triggering, overrange detection indicators, programmable gains, filters and signal conditioning. Input modules are compatible with the company's higher-speed ac- and dc-powered systems, supporting up to 256 channels. An integrated, menu-driven window-oriented software package, called Test Control Software, speeds test setups, equipment verification, and data analysis. The software can export results to formats such as binary, floating point, and ASCII for use with third-party software. The 3108AC mainframe, with TCS software, costs $7995. Modules cost from $100 to $1000 per channel depending on functionality. Delivery is in 4 to 6 weeks.

***Optim Electronics Corp.***
*Middlebrook Technology Park*
*12401 Middlebrook Rd.*
*Germantown, MD 20874*
*(301) 428-7200*
**▶ CIRCLE 724**

### ▼ 16-BIT DATA LOGGER TAKES 100-V DC INPUTS

The Model DT505 Datataker series, 16-bit data logger accepts measurements from a wide range of sensors and handles input voltages to 100 V dc with no need for external attenuators. A built-in memory card slot accepts memory cards with a capacity of up to 170,000 readings. The unit scans up to 30 analog, four counter/digital, and two high-speed counter channels at sample rates to 25 channels/second. Stored data can be unloaded by any personal computer in RS-232 ASCII format. The instrument comes with IBM-compatible software, and control commands are in simple English-language format. The DT505 costs $3967. A DT605 version, which includes a built-in LCD display, costs $4560. Both are available from stock to 2 weeks.

***Science/Electronics Corp.***
*P.O. Box 986*
*Dayton, OH 45401-0986*
*(800) 543-9930 or (513) 859-5555*
**▶ CIRCLE 725**

### ▼ ANALOG INPUT BOARD FEATURES ON-BOARD DSP

The PC-1601 series analog-to-digital plug-in boards for IBM PC/AT-compatible computers incorporates a digital signal processor to perform a variety of complex tasks not readily handled by other analog-to-digital boards. The boards sample at 330 samples/second. The PC-1601A has a 16-channel multiplexer and comes with user-interface software and a DSP assembler, linker, and simulator to create DSP resident functions. An optional Turbo C++ command library helps to create custom programs that use factory-loaded DSP resident functions. The PC-1601A sells for $1485.

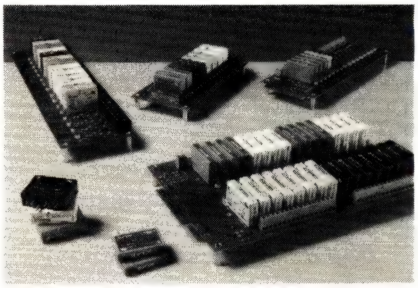
***Omega Engineering Inc.***
*1 Omega Dr.*
*Stamford, CT 06907-4047*
*(203) 359-1660*
**▶ CIRCLE 726**

### ▼ SOFTWARE SPEEDS TEST PROGRAMMING IN C

LabWindows/CVI (C for virtual instrumentation) helps users develop instrumentation applications in either the ANSI C programming language under Windows for PCs or under Solaris for Sun Sparcstations. The software supplies automatic code-generation for users who want to employ traditional programming tools. LabWindows/CVI includes an ANSI C compiler, linker, debugger, variable trace display, and memory checking capabilities. Also in the package are libraries for performing data acquisition, analysis, and presentation and more than 300 GPIB, VXI, and RS-232 instrument drivers. Programs developed with LabWindows/CVI are completely portable between Windows and Solaris operating systems. The LabWindows/CVI full development system for Windows costs $1995. A base package, which does not include the Advanced Analysis Library, costs $995. A LabWindows/CVI VXI development system for Windows sells for $3995. LabWindows/CVI for the Sun will be available in December for $3995 for a single-user, floating license. The LabWindows/CVI VXI development system for the Sun will cost $4995. Existing LabWindows users can upgrade to the Windows version of LabWindows/CVI for $495 and the Sun version for $2495.

***National Instruments Corp.***
*6504 Bridge Point Pkwy.*
*Austin, TX 78730-5039*
*(800) 433-3488 or (512) 794-0100*
**▶ CIRCLE 727**

### ▼ ISOLATED I/O MODULES OFFER 4000-V PROTECTION



The SCMD series of I/O modules and accessories create a 4000-V protective isolation barrier devices in the field and the host computer. The result is a safe interface for industrial measurement and control applications. The input modules accept 18 to 230 V ac in three ranges and 3.3 to 60 V dc in two ranges. They convert the voltages to dc logic signals and send them to the computer. The output modules accept 5-, 15-, or 24-V dc signals from the computer and use these voltage commands to switch ac or dc circuits on and off. Full-size modules or 0.6 in. wide, and miniature versions are 33% thinner and 20% shorter for increased density. The modules are approved by Underwriters Laboratory and the Canadian Standards Association. They cost from $8.10 to $9.35 in lots of 100 and are shipped from stock.

***Dataforth Corp.***
*2731 E. Elvira Rd.*
*Suite 171*
*Tucson, AZ 85706*
*(602) 741-1404*
**▶ CIRCLE 728**

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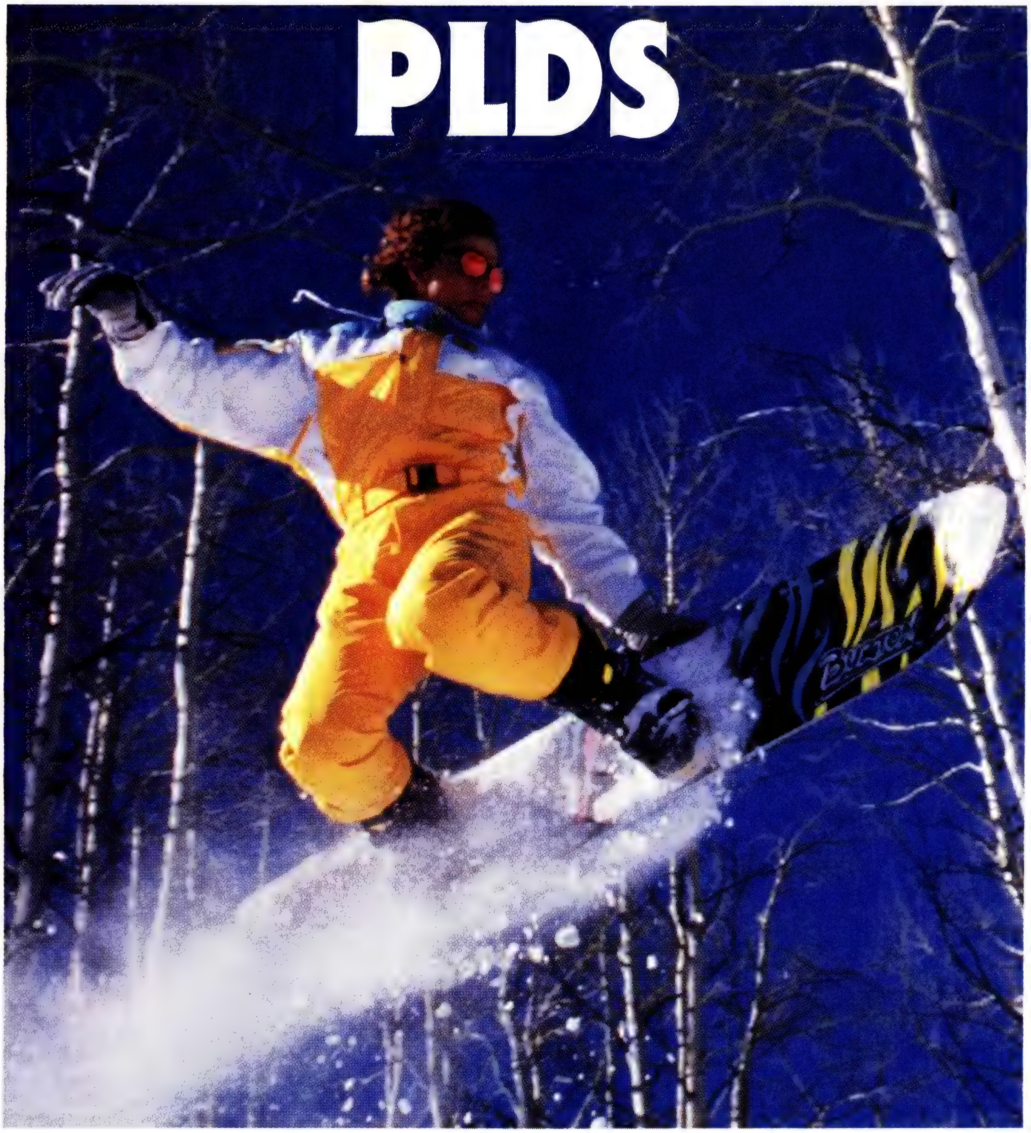

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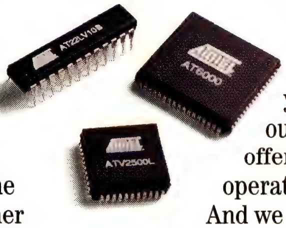

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CIRCLE 216 FOR U.S. RESPONSE CIRCLE 217 FOR RESPONSE OUTSIDE THE U.S.

### ▼ FAST I/O BOARDS BOAST 12-BIT RESOLUTION

A pair of high-performance analog and digital I/O boards for IBM-compatible PCs offer sampling rates to 100,000 samples/second with DMA transfers. The boards feature eight differential or 16 single-ended analog inputs with 12-bit resolution. The DAS-1201 supplies gains of 1, 10, 100 and 500 at speeds to 50,000 samples/second. The DAS-1202 offers gains of 1, 2, 4, and 8 at up to 100,000 samples/second. Also available are 32 digital I/O channels. Included is Basic software needed to operate the boards. An advanced software option, ASO-1200, supplies drivers for programing in the Windows environment and under DOS using C or Pascal. The DAS-1201 and DAS-1202 cost $449, and the ASO-1200 costs $99. Delivery is from stock.

***Keithley MetraByte***
*440 Myles Standish Blvd.*
*Taunton, MA 02780*
*(508) 880-3000*
**▶ CIRCLE 729**

### ▼ SOFTWARE LINKS LABVIEW WITH DATABASES

Users of National Instruments' LabView graphical instrumentation software can now use a virtual instrument (VI) library to access databases residing on VAX, VMS, and AS/400 computers. Called Lab.dbf, the library employs a variety of networks—including Novell, NetBIOS, TCP/IP, DECnet, and AppleTalk—to transfer data. Operators need no knowledge of the network or database. To store data, they connect to the server and log onto the database, which is similar to opening a file. They then pass data to the Database Write VI, which handles all networking and protocol needs automatically. After the transfer, another VI closes the connection to the server. Lab.dbf for Windows-based PCs and Macintoshes costs $500.

***Porter Consulting***
*85 Casey St.*
*Norwood, MA 02062*
*(617) 769-3752*
**▶ CIRCLE 730**

### ▼ INTERFACE CARD MEETS IEEE-488.2 STANDARD

The Model 488-PC2 IEEE-488 bus interface card has been improved to bring it up to the IEEE-488.2 standard, and other enhancements also have been added. The upgraded interface board, which operates in any IBM-compatible ISA-bus computer, includes driver libraries for the four most popular programming languages and is compatible with the newer instruments that use the Standard Commands for Programmable Languages. Interrupt processing has been improved for real-time control of devices on the IEEE-488 bus and the DMA transfer rate also has been increased. The new board is backward compatible with the older versions of the interface. The 488-PC2 costs $345, and delivery is from stock to 2 weeks.

***ICS Electronics Corp.***
*473 Los Coches St.*
*Milpitas, CA 95035-5545*
*(408)-263-5500*
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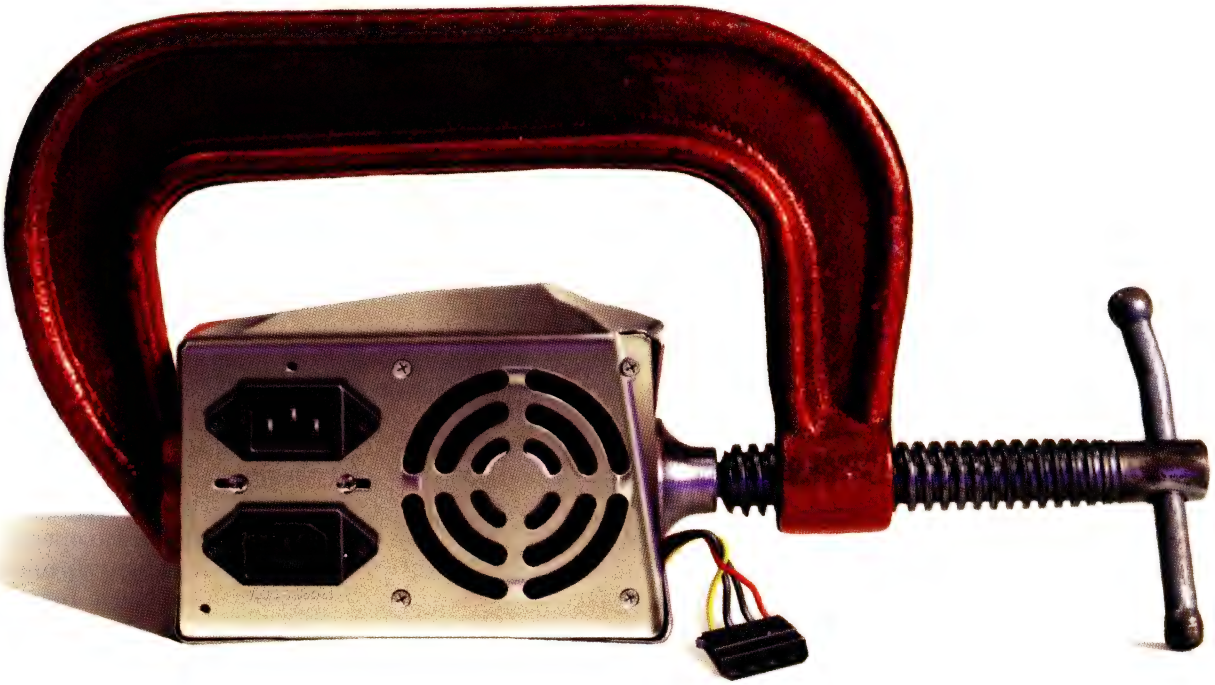

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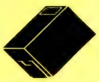
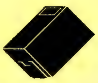
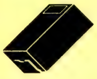
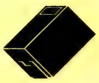
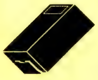
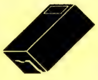
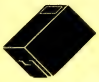
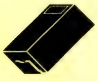
|  | | |  |  |  |  | |  |  |  |
| 6.3 V | 10 V | | 16 V | | 20 V | | 25 V | | 35 V | |
| 330 µF | 220 µF | 100 µF | 100 µF | 47 µF | 68 µF | 33 µF | 33 µF | 22 µF | 22 µF | 10 µF |
| 100 mΩ ESR | 100 mΩ ESR | 100 mΩ ESR | 100 mΩ ESR | 150 mΩ ESR | 150 mΩ ESR | 200 mΩ ESR | 200 mΩ ESR | 300 mΩ ESR | 300 mΩ ESR | 300 mΩ ESR |
| D case size = EIA 7343 E case size = EIA 7343H | | | | | | | | | | |

CIRCLE 218 FOR U.S. RESPONSE CIRCLE 219 FOR RESPONSE OUTSIDE THE U.S.

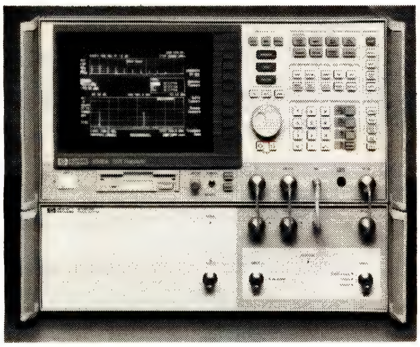
### ▼ EMULATOR ADDS MIDRANGE SUPPORT FOR 80C186

The CodeTAP-XA (extended architecture) emulator adds a third level of support for Intel's 80C186 series microcontrollers. The CodeTAP-XA fits in between the EL 1600 full-scale emulator and the lower-priced CodeTAP emulator. In addition to basic emulator features—such as 20-MHz no-wait-state operation, source-level execution trace, hardware and software breakpoints, source-level debugging, and high-speed communications—CodeTAP-XA offers a complex sequential event system, real-time trace capability with event system qualification and display without stopping emulation, overlay memory of 256 kbytes or 1 Mbyte, and performance analysis. CodeTAP-XA is fully integrated with the Paradigm Debug interface and supports Borland and Microsoft C/C++ and Microtec Research compilers running on 386-based or above PCs. CodeTAP-XA costs from $7495 to $8495, depending on configuration. Paradigm Debug costs $1495. Delivery is in 4 to 6 weeks.

***Applied Microsystems Corp.***
*5020 148th St.*
*Redmond, WA 98073-9702*
*(800) 426-3925 or (206) 882-2000*
▶ **CIRCLE 732**

### ▼ EMI RECEIVER PERFORMS COMPLIANCE TESTING

The HP 8546A EMI compliance receiver conforms with CISPR Publication 16 recommendations for meeting worldwide commercial electromagnetic interference measurement (EMI) standards. The receiver features a 9-kHz-to-6.5-GHz frequency range; 200-Hz, 9-kHz, and 120-kHz CISPR bandwidths; and a 10-dB characteristic noise figure. Absolute amplitude accuracy from 9 kHz to 1 GHz is ±2 dB. Features include built-in limit lines; automatic measurement routines; a PC-formatted floppy disk drive; manual, step, and scanning tuning modes; and peak, quasi-peak, and average parallel detectors. The receiver consists of two sections. The HP 85462A RF receiver can be bought as a stand-alone pre-compliance tester. The HP 85460A RF filter section can be added later. The HP 8546A costs $65,000, the HP 85462A $38,000, and the HP 85460A $27,000.



***Hewlett-Packard Co.***
*Direct Marketing Organization*
*P.O. Box 58059*
*MS51L-SJ*
*Santa Clara, CA 95051-8059*
*(800) 452-4844*
▶ **CIRCLE 733**

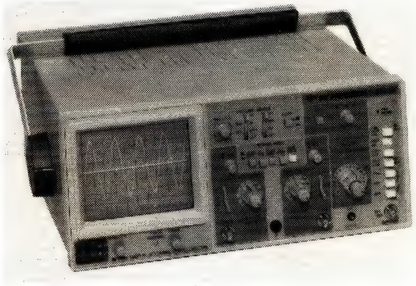
### ▼ $I_{DDQ}$ TEST SOFTWARE NEEDS NO DFT STRUCTURES

Designers who are unable or unwilling to accept the silicon overhead of design-for-test structures such as scan cells can use CurrenTest, a test development software solution for $I_{DDQ}$ testing. The software uses a proprietary technique to automatically select and grade a limited set of functional vectors for fault coverage. This vector selection, performed on a full set of user-provided functional vectors, minimizes test time. It also avoids operational conditions that might cause excessive $I_{DDQ}$ leakage, which would create false "fault" indications. CurrenTest is available on Sun Sparcstation and Sparcserver platforms. Prices range from $25,000 to $45,000, depending on fault model options and configurations.

***CrossCheck Technology Inc.***
*2833 Junction Ave.*
*Suite 100*
*San Jose, CA 95134*
*(408) 432-9200*
▶ **CIRCLE 734**

### ▼ 20-MSAMPLE/S DSO OFFERS ANALOG CAPABILITY

The advantages of both analog and digital storage oscilloscopes are available in the 2-channel Model 2522A. In the digital mode, the portable scope offers 20 Msample/s real-time sampling on each channel and an equivalent-time (repetitive) bandwidth of 20 MHz. Memory in real-time operation is 2 ksamples/channel. Using repetitive sampling, memory is 1 ksample/channel. Vertical resolution is 8 bits. The digital display modes include roll, refresh, hold, save channel 2, and pretrigger storage. The analog mode delivers 20-MHz dual-trace operation with a vertical sensitivity up to 1-mV/div. It also has a V-mode for viewing two signals that are unrelated in frequency. The 2522A portable scope comes with two 10:1 probes for a suggested user price of $1099.



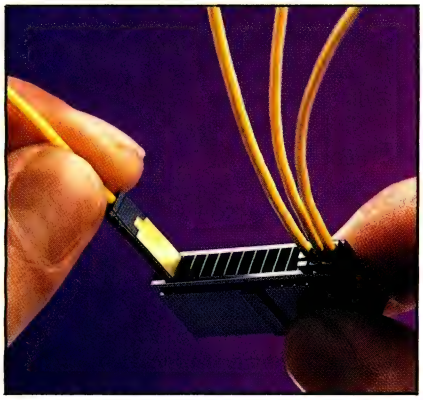
***B+K Precision***
*Maxtec International Corp.*
*6470 W. Cortland St.*
*Chicago, IL 60635*
*(312) 889-1448*
▶ **CIRCLE 735**

### ▼ DEVELOPMENT SYSTEM AIDS RISC DESIGNERS

STEPGuide is an integrated, interactive development environment for embedded RISC systems. Based on a point-and-shoot Windows environment, the package of tools helps designers from the code-generation stage through emulation, debug, and real-time measurement. System functions include cache reconstruction; non-intrusive examination of activities in RISC processors that can be running at up to 50 MHz; concurrent viewing of compilation errors, source and assembly; and execution reconstruction. The processors that are supported include AMD's 29K family, Intel's 960 devices, and Fujitsu's Sparclite. All of STEPGuide development system's facilities are accessed through its graphical user interface. STEPGuide prices range from $3000 for the basic software platform to $35,000 for the complete hardware and software package.

***Step Engineering Inc.***
*661 E. Arques Ave.*
*Sunnyvale, CA 94088-3166*
*(800) 538-1750 or (408) 733-7837*
▶ **CIRCLE 736**

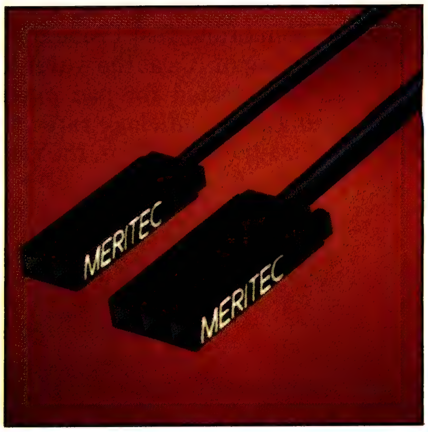
### CONTROLLED IMPEDANCE GROUND PLANE INTERCONNECTS (GPI$_{TM}$)



Meritec's new Ground Plane Interconnects are engineered to match impedance and propagation rate while minimizing crosstalk. The assemblies are impedance matched from the board through the assembly. As a result, signal-to-signal crosstalk is minimized. The assemblies are designed for CMOS, ECL orGaAslogic.Aspringlatch connects the termination to the housing or to Meritec's Single Signal Carrier System (SSC$_{TM}$), which allows grouped interfacing with single, dual or triple row headers. Precision, high strength molded terminations are highly reliable in critical applications.
**Circle No.224**

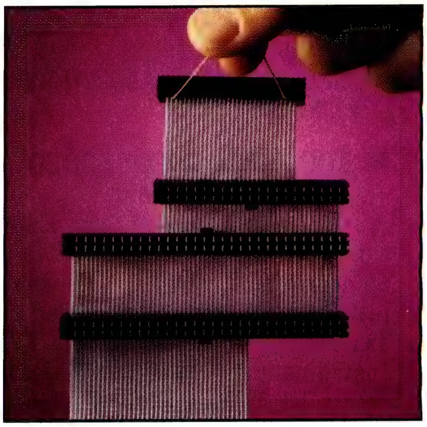
### Single Signal Interconnects Offer High Performace in a Subminiature Package

Meritec's economical 1x2 and 1x3 Single Signal Interconnects (SSI$_{TM}$) are designed for .100" x .100" applications using sub- miniature coax cable. The assemblies are engineered to match application requirements for controlled impedance and propagaion rate while minimizing crosstalk. The assemblies are designed for CMOS, ECL or GaAs logic. A spring latch connects the termination to the housing or to Meritec's Single Signal Carrier Systems (SSC$_{TM}$), which allow grouped interfacing with single, dual or triple row headers. Precision, high strength molded terminations are highly reliable in critical applications. Boxed contacts with thermo resistance welding provided the ultimate in electrical continuity.**CIRCLE NO.225**



### Multi Signal Interconnects for TTL Fast and Fast CMOS Logic

Meritec's controlled impedance Multi Signal Interconnects (MSI$_{TM}$) are designed fo TTL fast and fast CMOS logic. The high performance assemblies are available in standard end-to-end terminations or can be daisy chained for spacial applications. Abrasion-resistant jacketing and EMI/RFI electrical shielding are optional. The connectors mate with standard .025" square or round pins on a .100" grid. Precision, high strength molded terminations provide high reliability in critical applications.
**Circle No.226**



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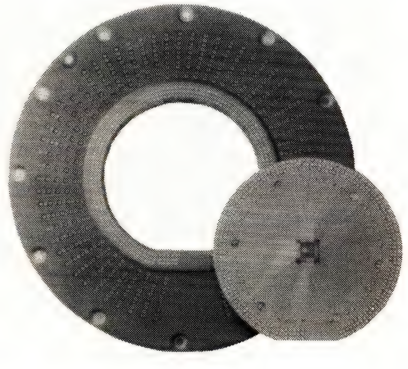
**CIRCLE 222 FOR U.S. RESPONSE**

**CIRCLE 223 FOR RESPONSE OUTSIDE THE U.S.**

## ▼ MEMBRAME PROBE TESTS ICs AT WAFER LEVEL

The IC Membrane Test Probe for at-speed testing of ICs at the wafer level has been tested for pad pitches down to 4 mils and clock rates to 2 GHz. During beta testing, the probe achieved more than 350,000 touchdowns in at-speed wafer-level tests. The probe delivers controlled impedance paths from the probe card interface to the die surface with line-to-line isolation of better than 30 dB. The probe consists of a universal rigid probe ring that conforms to the specific tester in use and a flexible membrane customized for the target IC. Prices vary but a probe for an advanced 32-bit microprocessor with more than 120 pins costs less than $3000. Delivery takes 8 weeks for a customized pad layout but reorders are filled in 4 weeks.



***Packard-Hughes Interconnect***
*17150 Von Karman Ave.*
*Irvine, CA 92714*
*(800) 821-2998 or (714) 660-5701*
▶ **CIRCLE 737**

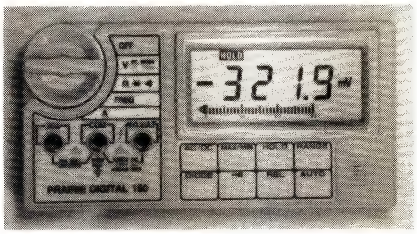
## ▼ TOOL SPEEDS EMBEDDED TEST DEVELOPMENT

A software tool called Scan Engine simplifies the application and development of test programs or vectors in systems requiring embedded test. The software works with the Texas Instruments SN74ACT8990 test bus controller chip to perform go/no-go built-in self tests that can be accessed by field service personal. Scan Engine supports any kind of test that can be initiated and executed with boundary scan, including interconnect, functional, device, or logic-cluster testing. The software is portable ANSI C source code that reads serial scan vectors from memory and applies the test procedures to the system. Source code is provided so that Scan Engine can be compiled and run on almost any microprocessor. Scan Engine carries a license fee of $12,000 plus royalties.

***Texas Instruments Inc.***
*Literature Response Center*
*P.O. Box 172228*
*Denver, CO 80217*
*(800) 477-8924 ext. 3801*
▶ **CIRCLE 738**

## ▼ HANDHELD DMM OFFERS SERIAL PORT, TRUE RMS

The Model 150-02 is a handheld true RMS digital multimeter with an RS-232 serial port for both data output and instrument control. The full-function meter can be connected to any computer with an RS-232 port, but it comes with an IBM PC-compatible cable and DOS software. The software logs readings to the screen, printer, or a disk data file. The interval is programmable, and readings can be time and date stamped. Measurements include true RMS ac voltage and current, dc voltage and current, resistance, continuity and diode tests, and frequency from 30 Hz to 400 kHz. A 12-bit analog-to-digital converter offers a full-scale count of 3999 (3-3/4 digits). The optoisolated RS-232 interface provides 2000 V of isolation to protect the host computer. The 150-02 costs $179.



***Prairie Digital Inc.***
*846 17th St.*
*Prairie du Sac, WI 53578*
*(608) 643-8599*
▶ **CIRCLE 739**

## ▼ LOWER-COST TESTER HANDLES VLSI DEVICES

The J971LC is designed for economical production test of high-performance VLSI devices. The tester is a lower-cost version of the J971, with which it is program compatible. The J971LC tests devices with up to 384 pins at speeds to 50 MHz with an edge placement accuracy of ±700 ps. The J971LC can do parallel testing (multiple devices tested together on one system) and multiplexed testing (tests alternate between two test stations). A typical J971LC system costs between $600,000 and $1,000,000, about 25% to 30% less than a typical J971 tester.

***Teradyne Inc.***
*Semiconductor Test Div.*
*30801 Agoura Hills Rd.*
*Agoura Hills, CA 91301*
*(818) 991-2900*
▶ **CIRCLE 740**

## ▼ METERS MEASURE POWER DRAWN BY EQUIPMENT

A pair of power line meters help designers determine the precise power drawn by equipment under test in terms of RMS voltage and current, VA, instantaneous and reactive power, power factor, and accumulated power. Model PLM-1 monitors one nominal 120-V ac, 15-A output. PLM-2 has an additional rear-panel terminal strip that allows a combined 30-A measurement and flexibility in wiring configurations. An isolated RS-232 output can be used to transfer measurements as an ASCII string at 1200 bits/s. PLM-1 and PLM-2 prices range from $646 to $1038, depending on features selected. Delivery is in 4 to 6 weeks.

***Electronic Product Design Inc.***
*6963 Bluebelle Way*
*Springfield, OR 97478*
*(503) 741-0778*
▶ **CIRCLE 741**

## ▼ DEBUGGER HANDLES 68300, 68HC16 BACKGROUND MODE

The Xterminator, a background-mode debugger for Motorola's 68300 and 68HC16 processors, links the Motorola-standard debugging connector on the processors to a PC's parallel port. The unit comes with Softaid's Windows-based source-level debugger, SLD for Windows, so the Xterminator can debug any assembly or C language embedded program. The debugger non-intrusively accesses a target system's memory, registers, and I/O pins, and it supports an unlimited number of software breakpoints. The Xterminator with SLD for Windows costs $795 and is available from stock.

***Softaid Inc.***
*8300 Guilford Rd.*
*Columbia, MD 21046*
*(800) 433-8812 or (410) 290-7760*
▶ **CIRCLE 742**

### ▼ Z80182 EMULATOR RUNS AT UP TO 20 MHZ

The Model 8800 Emulator/Analyzer now performs 20-MHz, non-intrusive emulation on Zilog Z80182 designs. The Z182, which comes in 100-pin QFP and VQFP packages, is usually soldered onto a board. Consequently, two connection schemes are offered. Using the proprietary Clip-On Emulation method, designers clip onto the Z182 with a commercially available test clip. The other method bypasses the processor by connecting a flat ribbon cable from the emulation pod to a user-designed test header. The 8800 comes with symbolic debug and high-level language support. The 8800 Emulator/Analyzer for the Z182 starts at $10,500 with 64 kbytes of zero-wait-state emulation memory and a 16-kbyte trace buffer.

***Orion Instruments Inc.***
*180 Independence Dr.*
*Menlo Park, CA 94025*
*(800) 729-7700 or (415) 327-8800*
**▶ CIRCLE 743**

### ▼ SOFTWARE MANAGES EMI MEASUREMENT PROCESS

A family of PC-based software products manage the electromagnetic interference (EMI) measurement process. The HP 85877A commercial EMI measurement software simplifies conducted and radiated EMI testing. The HP 85875A software addresses conducted emission testing only; the HP 85876A software addresses radiated emissions. The software collects up to 28 predefined and 10 user-defined parameters for each signal encountered during test. The software runs on a 486-based PC with MS-DOS 5.0 or higher and Windows 3.1, and is compatible with most HP EMI receivers. The HP 85877A costs $13,000, the HP 85876A $9000, and the HP 85875A $6000.

***Hewlett-Packard Co.***
*Direct Marketing Organization*
*P.O. Box 58059*
*MS51L-SJ*
*Santa Clara, CA 95051-8059*
*(800) 452-4844*
**▶ CIRCLE 744**

### ▼ TESTER TARGETS FLASH MEMORIES, PCMCIA CARDS

The Wave family of Flash NVM memory test systems is specially designed to test Flash components, EEPROMs, nonvolatile RAMs, and Flash PLDs, as well as PCMCIA/JEIDA memory cards. A 64-device/32-card engineering model and 640-device/320-card production model are available. Both models come in ambient or environmental versions. The Wave is device-specific so every device is issued the correct number of write/erase pulses each cycle, preventing overprogramming or overerasure. Devices up to 256 Mbytes can be tested in 8-bit mode and up to 512 Mbytes in 16-bit mode. The unit features programmable power supplies and driver and comparator levels. Prices and delivery times vary depending on configuration.

***EPRO Corp.***
*3310 Victor Ct.*
*Santa Clara, CA 95054*
*(408) 982-9707*
**▶ CIRCLE 745**

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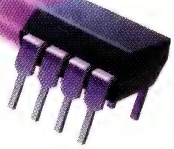
## Low harmonic distortion.

To reproduce your high-speed input signals with the greatest signal purity, choose from op amps such as the 350MHz CLC409, which delivers -65/-72dBc 2nd/3rd order harmonics at $2V_{pp}$, 100Ω, 20MHz. Plus a half dozen others with less than -50dBc distortion.

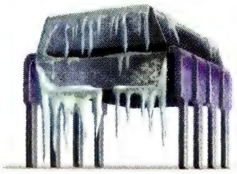
## Fast settling time.

Our wide range of high-speed op amps gives you a choice from 8-bit to 14-bit settling. They range from the 350MHz CLC409 with a fast 8ns to 0.1% to the 195MHz CLC402 with a blazing 18ns to 0.0025%.

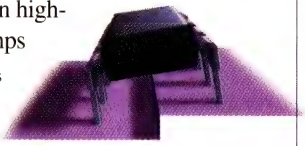


## Low power consumption.

Want high speed with low power? Choose from op amps like the 350MHz CLC409 with 135mW power dissipation, the 160MHz CLC406 at 50mW, the 300MHz CLC420 at 40mW, or the 50MHz CLC505 at 10mW, which lets you set supply current over a range of microamps to milliamps with a single resistor.



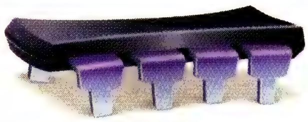
## Low offset voltage.



A half-dozen high-speed op amps give you $V_{OS}$ of less than 1mV. For example, the 1.7GHz GBW CLC425 delivers a low 100µV offset. The CLC402 and CLC409 provide $V_{OS}$ of 500µV. And nearly a dozen other fast op amps have less than 2mV offset.

## Low noise.

With its ultra-low $1.05nV/\sqrt{Hz}$ input noise, the CLC425 is the lowest-noise wide-band op amp on the market. Close behind is the unity-gain stable CLC426 with $1.4nV/\sqrt{Hz}$ input voltage noise. Followed by more than a dozen with $e_n$ less than $3.0nV/\sqrt{Hz}$.



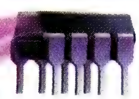
## Wide bandwidth.

Choose from our large family of dc-coupled wideband op amps. From the 55MHz CLC430 and the 350MHz CLC409 current-feedback op amps, to the 1.7GHz GBW CLC425 and the 5.0GHz GBW CLC422 voltage-feedback op amps.

## High gain.

Our large family of current-feedback op amps deliver nearly constant bandwidths over their gain ranges. For example, the CLC401, at a gain of +20V/V, gives a 150MHz -3dB bandwidth. And the voltage-feedback CLC422, with its 5.0GHz GBW, delivers the widest gain bandwidth product on the market.

## Fast slew rate.



Speed is our specialty, so you'd expect performers like the 175MHz CLC404, which delivers 2600V/µs and a $5V_{pp}$ output signal. Or the 200MHz CLC411, a 15V op amp at 2300V/µs. Plus nearly a dozen more with specs greater than 1000V/µs.

## Prices you can afford.

Pricing on our high-speed op amps is very competitive. And you'll find significant quantity discounts. Take a look, because we have dozens of fast op amps to choose from. Plus applications engineers that are ready to help you with product selection and design troubleshooting.

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CV4 8HX, England. Phone 44 203 422958, Fax 44 203 422961

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CIRCLE 234

# CODEC COMPRESSES IMAGES IN REAL TIME

## REAL-TIME MOTION VIDEO OR STILL IMAGES CAN BE COMPRESSED WITH SINGLE-CHIP MULTISTANDARD CODEC.

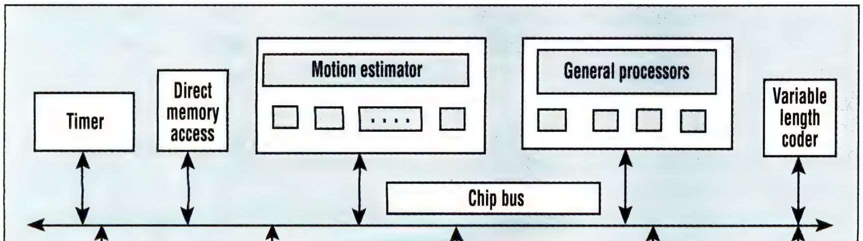
**DAVE BURSKY**

Until recently, real-time video compression at 30 frames/s required supercomputers to do all of the computations. However, over the last year improvements in integration and algorithms reduced the processing subsystem to just a few complex VLSI chips and some support circuits. Now, with the release of the CL4000 from C-Cube Microsystems, a single VLSI chip can perform real-time video encoding or decoding for full compatibility with the MPEG (Motion Picture Experts Group), Px64 image-compression, and JPEG (Joint Photographic Experts Group) standards.

Though other companies are closing in on the same target, the CL4000 is the first commercial chip to perform encoding and decoding for all of the standards on the same piece of silicon. Such a level of integration could drastically lower the overall price of multimedia authoring subsystems to less than $4000 within a year or two. This would, in turn, allow more companies to begin developing multimedia-related applications or apply the chips to applications such as high-definition TV.

To do the computations, designers at C-Cube put an almost unheard of amount of horsepower on the chip by using 1.2 million transistors. Those transistors are applied to different functional and computational blocks that are set up as independently controlled blocks tied together by a common internal bus *(Fig. 1)*.

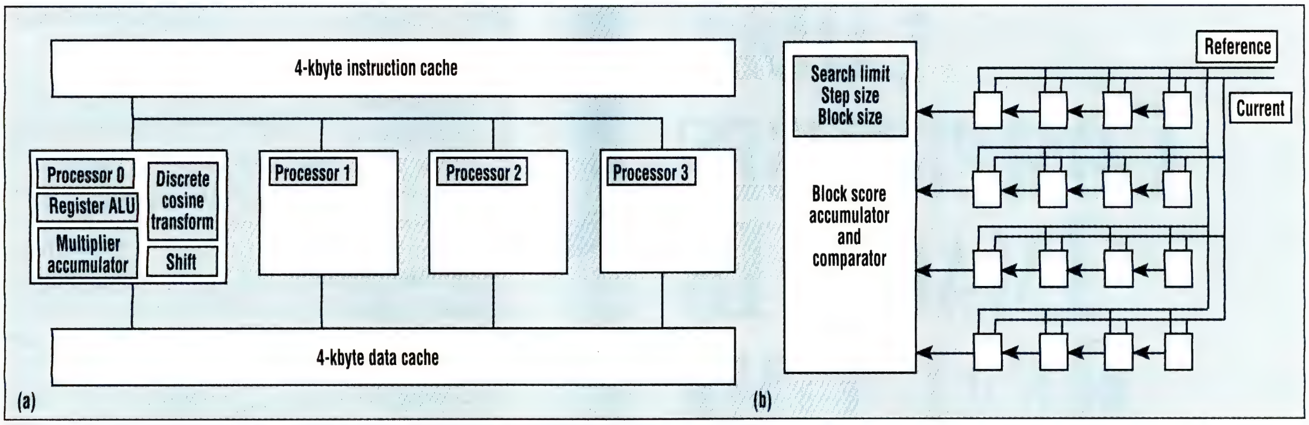
With the large amount of horsepower imbued on the chip, the CL4000 can perform real-time MPEG encoding or decoding of 352-by-240-pixel images at rates of up to 30 frames/s (or 320 by 288 pixels at 25 frames/s), become a Px64 full-duplex codec for 352-by-288-pixel images at up to 15 frames/s, and perform JPEG image compression or decompression. More basic functions also whiz by—an 8-by-8 element discrete cosine transform (DCT) and quantization needs just 200 clocks (at 16.5 ns/clock), while a motion sense estimation on two 16-by-16-pixel blocks is just 70 clocks.



**1. EXECUTING OVER 2450 MOPS,** this single chip image compression/expansion processor, the CL4000 from C-Cube Microsystems, employs a central bus over which all internal processor sub-units transfer their data. The two key blocks on the chip include the Motion Estimator, which runs at about 2000 MOPS, and the other block is the general-purpose processor section that runs at about 240 MOPS.

Furthermore, multiple CL4000s can be employed in unison to encode even larger, high-resolution images—720-by-480 pixels at 30 frames/s. With Px64 (also referred to as H.261), The codec can perform quarter CIF (compressed image file) and full CIF image encoding and decoding, half-duplex encoding (CIF with a 15-Hz clock) and half-duplex decoding for compressed image files with frame rates of 30 and 10 Hz, respectively.

To handle such operations with overhead to spare, the chip runs its internal clock at 60 MHz—that translates into a chip power dissipation of 4.5 W when powered by a 5-V supply. The system throughput gets its first contribution of 240-million-operations-per-second (MOPS) from a gen-



**2. THE GENERAL-PURPOSE PROCESSOR BLOCK** **actually contains four 32-bit CPU cores, each of which has access to a shared 4 kbytes of instruction cache and 4 kbytes of data cache (a). To perform motion estimation, the estimator sub-block employs 16 subprocessors arranged in a SIMD architecture to process 16 pixels (in a 4-by-4 array) at a time (b).**

eral-purpose compute engine composed of four identical 32-bit subprocessors *(Fig. 2a)*. Those subprocessors are organized as a simple array processor employing a single-instruction, multiple-data (SIMD) architecture. The four processors share 4 kbytes of instruction cache and 4 kbytes of data cache.

Also included on the chip is a 2000-MOPS motion estimator with 16 subprocessors and control logic. The subprocessors are arranged in a four-by-four matrix (to handle 16 pixels at a time) that also executes SIMD operations *(Fig. 2b)*. The estimator searches for half-pixel motion vectors and has programmable search range and block size, permitting the user to optimize the search and computation algorithms.

The rest of the chip contains a 50-MOPS video interface to transfer all video data, a variable-length encoder and decoder, and an 80-Mbyte/s DRAM controller (for image storage) with a timer and a direct-memory-access (DMA) controller. The video-interface blocks give designers the option to interpolate output video data, or use the ports on those blocks for high-speed data. A seven-tap decimation filter is also available to preprocess input video pixels.

In the variable-length encoder, the circuitry reorders discrete-transform coefficients, counts runs of zeros, performs Huffman encoding of run-value pairs, includes Huffman tables for Px64 and MPEG encoding schemes (stored in ROM), and supports tables in RAM for other encoding standards. The decoder is ROM based and performs Huffman decoding based on CPU commands. Run-value pairs are also expanded and reordered by the decoder.

To aid in board-level testing and emulation, the chip can be accessed over an IEEE-compatible 1196 JTAG test port. A typical board design for NTSC systems would include the CL4000, both an NTSC decoder and an encoder, a pair of 4-Mbit DRAMs, and some bus interface logic. On the chip are four data-transfer buses and a total of 168 leads on a ceramic pin-grid array. Also on the chip are a 32-bit non-multiplexed host interface with NuBus-type control signals, a high-speed memory-bus interface with integrated DRAM controller that addresses 2 Mbytes of local DRAM, a DMA controller, and video input and output ports. The host bus handles processor initialization and control, compressed-data transfers, input and output, and multichip interprocessor communications.

One CL4000 can perform CIF-quality encoding, which is desktop computer/PC-oriented; to perform DCTs, two of the CPU cores must be used in tandem, leaving only two CPUs for general use. If a pair of CL4000s are used, they can deliver SIF-quality video and CD-quality audio, good enough for most authoring systems. For ultimate quality, boards with from 8 to 10 CL4000s deliver NTSC (8 chips), PAL (10 chips), and CCIR 601 encoding with studio-quality real-time throughput.

Development tools include a symbolic debugger, an X-windows graphical user interface (for remote sessions), Sparc-hosted tools, and a VME card target development system. A microcode assembler delivers both compiler output and assembly source. The Gnu C compiler is also part of the source software and supports in-line assembly and a symbolic debugger. A full suite of microcode libraries for image processing include a run-time kernel, video processing, host services, diagnostics, and profiling. C-Cube host software includes a demo application, host driver, microcode download and chip initialization, and diagnostics.

Hardware support starts with the CLM4610, a development card that supports up to six CL4000s and goes up to a seven-slot VME chassis into which a Sparc CPU is added to ease software-development turn-around. A Video input card provides a parallel D1-format digital input and connects to the encoder card through the P2 VMEbus connector.☐

### PRICE AND AVAILABILITY

*The CL4000 codec chip is immediately available. In single quantities, the CL4500 chip set for SIF encoding including software drivers costs $4000. The CL4600 chip set for broadcast-level MPEG encoding including software drivers costs $10,000.*

*C-Cube Microsystems Inc., 1778 McCarthy Blvd., Milpitas, CA 95035; Rick Rasmussen, (408) 944-6300.* **CIRCLE 511**

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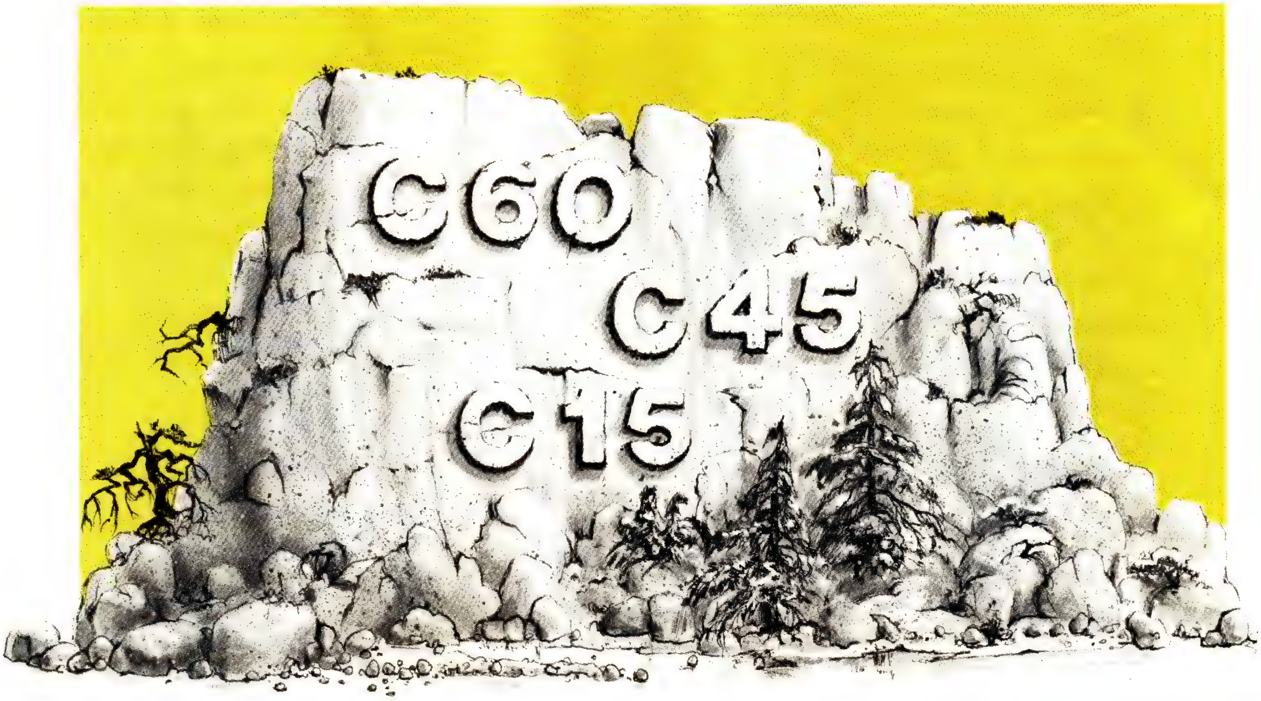

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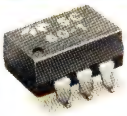
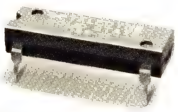
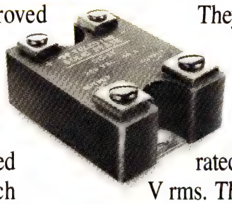

*Surface Mount Shown*

Housed in a 6 pin mini-DIP, the C60 Series is a family of bi-directional FET output solid state relays capable of controlling ac, bi-directional or dc loads. The optically coupled C60 handles a broad range of switched voltages (up to ±360 Vdc) and currents (up to 1.0 Arms /2.0 Adc). The unique three terminal output allows the user to parallel the output FETs externally for dc operation ensuring low on resistance down to 0.075 ohms.

### C45

The C45 has a significantly improved price/performance ratio. This series of solid state ac relays are optically isolated. The units contain back-to-back photo SCRs and a zero crossing circuit developed by Teledyne. The tight zero switch window ensures reliable transient free switching of AC loads and very low EMI and noise generation. The optical isolation of control from output affords noise free power switching. This series can switch from 10 ma to 1.0 amp rms at 250 Vrms. The C45 is packaged in a low profile 16 pin DIP package.





### C15

The C15 ac solid state relays are truly valued engineered, employing back-to-back SCRs with a zero crossing turn on circuit. They also provide transient free switching of AC loads and very low EMI and noise generation. This series of solid state relays has versions rated from 10 to 40 amp rms at 250 V rms. These units are packaged in the familiar industry standard configuration.

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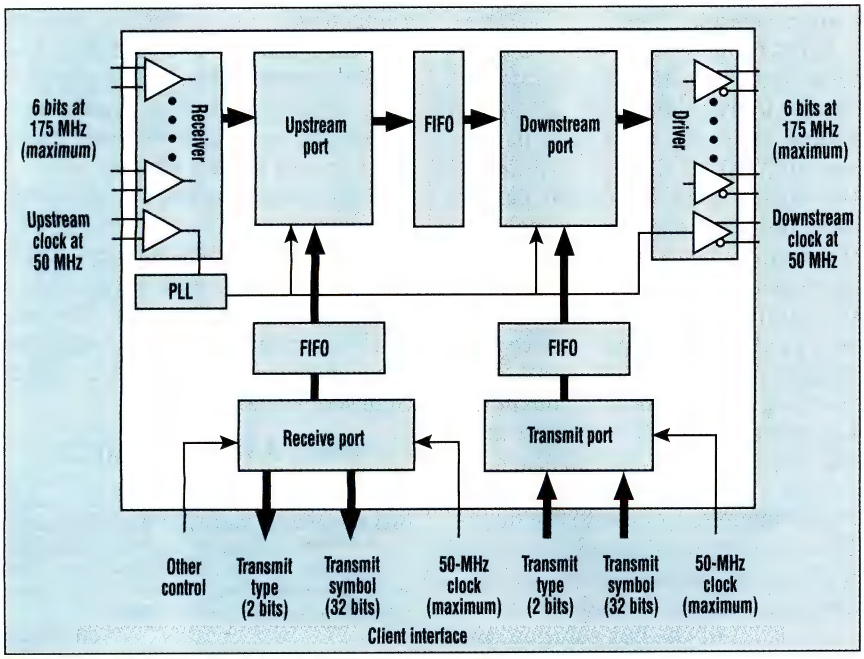
### SINGLE-CHIP SOLUTION SENDS DATA AT HIGH SPEEDS EITHER FROM CARD TO CARD OR SYSTEM TO SYSTEM.

# IC PASSES 350 MBITS/S THROUGH RING ARCHITECTURE

**RICHARD NASS**

In a typical computer configuration, data is passed to peripherals by sending the data to the CPU. The CPU deciphers the information and then sends it to the appropriate target. At times, though, it's more beneficial to pass data directly from one peripheral to another. This particularly holds true when large blocks of data are being transferred, such as in graphics-intensive applications or when using a disk array or other large mass-storage device.

By using a ring architecture, data can be passed sequentially from device to device without having to get "permission" from the CPU. A new implementation called QuickRing is one such example of the ring architecture. QuickRing can pass data at 350 Mbits/s to up to 16 nodes (transmit/receive points), either within the system or to a nearby (within 3 m) external peripheral. It can also transmit non-overlapping streams concurrently, each at the ring's maximum speed. In other words, node two can send data to, say, node four while node six is sending data to node eleven.



**1. RING AND CLIENT INTERFACES comprise the QR0001 QuickRing controller. The ring interface, which connects to other nodes in the system, has an upstream port for arriving data and a downstream port for departing data. Each module's upstream port is connected to the downstream port of the next module in the sequence. The client interface, which talks to the peripheral it resides on, has a transmit port for locally generated data streams and a receive port for locally absorbed streams.**

Bus-type architectures are suited for many typical computer operations, where various unrelated units of data from different memory locations are called from memory and manipulated before returning to their memory location. However, for blocks of stream-oriented data in which a beginning address is followed by large chunks of data, a sequential communications path or ring is more suitable. QuickRing sends data in streams of packets, with only the first packet carrying an address. With its efficient handling of data streams, this technique is particularly applicable in digital video and other applications with "infinite" data streams.

To implement QuickRing, one controller circuit must reside on each node. The single-chip QR0001 QuickRing data-stream controller, developed by National Semiconductor Corp., streams 350 Mbits/s simultaneously using both edges of a 175-MHz clock. The 350-Mbit/s transfer rate comes from the fact that one bit is taken on each edge of the ring's 175-MHz clock.

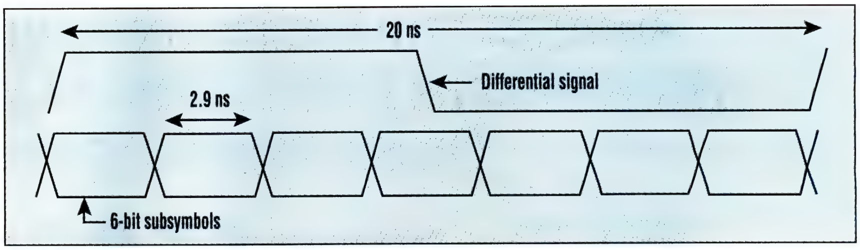
The same QuickRing IC is placed on every node, including the master. One of the chip's pins is tied high or low to indicate whether the device is a master or slave. Each ring can have up to 16 nodes, but only one master.

Basically, QuickRing's main role consists of pipelining data streams. It's logically equivalent to placing a large FIFO buffer between each node. As one node stuffs the FIFO with data, the next node extracts it. Then, either the data is used or it's stuffed into the following buffer.

The controller is built with two interfaces, a ring interface and a client interface *(Fig. 1)*. Each contains two unidirectional ports so that incoming and outgoing data can be queued simultaneously. One of the ring-interface ports, the upstream port, is used for arriving traffic, while the downstream port handles the departing traffic (the ring interface forms the link to other nodes in the network). The upstream port of each module is connected to the downstream port of the next module in the sequence. The interface is implemented using differential drivers and receivers.

In the client interface, the transmit port handles any locally generated data streams, while the receive port takes care of the locally absorbed streams. The two ports each possess a 32-bit data path with TTL-compatible I/Os and separate clock and control signals. The client interface links to the board or peripheral in which the QR0001 physically resides.

The ring carries one 42-bit symbol every 20 ns. The symbol consists of 32 data bits, 7 error-correction and detection bits (an internal Hamming-code algorithm implements single and double error correction), 1 frame bit, and 2 control bits. For transmission, the symbol is divided into seven subsymbols of 6 bits. The controller then multiplexes the subsymbols onto the six differential signal pairs on the downstream port *(Fig. 2)*. A seventh differential signal, with a 50-MHz (maximum) clock, accompanies every 42-bit stream.



**2. QUICKRING CAN SEND ONE** 42-bit data stream every 20 ns. For transmission, the stream is divided into seven 6-bit subsymbols. Those subsymbols are then multiplexed onto six differential signal pairs on the downstream port. A seventh differential signal, with a 50-MHz (maximum) clock, accompanies every 42-bit stream.

When the system is powered up, the master initiates the setup sequence. First, it identifies how many nodes are on the ring. Then it sequentially assigns an address to each node. The master is always assigned address 0. This address is stored internally within each controller chip. The master's power-on sequence is self-generating—no external CPU is needed. All of the configuration utilities are stored on the chip using state-machine logic. Once the initialization is complete, the master sends a data stream around the ring, telling each node that initialization is complete and normal data transmission can begin.

QuickRing uses a voucher-ticket technique to identify when a node is ready to receive data. Before a source node can send data, permission to transmit must be granted by the target node. To obtain permission, the source sends a voucher to the target. The target then grants permission by returning a ticket to the source. This can only be done on receipt of a voucher (the source must initiate the transfer of data). When the target receives the voucher, it has two options: absorb the voucher and return a ticket; or return the voucher. If the source receives a ticket, it transmits its data to the target. If it receives a returned voucher, it waits and retransmits the voucher to the target after 100 clock cycles.

In an out-of-the-box solution, various cabling technologies have been tested (such as copper) in 1- and 3-m lengths, which is adequate for the intended applications. National Semiconductor plans to test up to 10 m.

Popular QuickRing applications will find their way into the networking arena, such as hubs and routers. Currently, designs for the Macintosh are ahead of those for the PC because Apple has been one of the main forces behind the technology. Another application in the works is a multiprocessor system, where the ring is used to pass large amounts of data from one processor card to another.

One lingering problem that must be addressed involves the failure of a QuickRing node. If a node fails, it brings down the entire ring, just as most failures within a computer will halt operations. Error-detecting code is included on the chip, but for a higher-level failure (such as a node going down), the overlying system software would have to detect and handle the situation. There needs to be a certain amount of intelligence within the operating system, using some type of polling system.

Aside from handling the node-failure problem, future-generation QuickRing parts will be more application-oriented. For example, a broadcast feature, useful for networking, would allow all nodes to receive data simultaneously, rather than sequentially.☐

### PRICE AND AVAILABILITY

*The QR0001 ICs are currently sampling, with production expected to commence sometime in the fourth quarter. In quantities of 10,000, prices range from $30 to $40.*

*National Semiconductor Corp., 2900 Semiconductor Dr., P.O. Box 58090, Santa Clara, CA 95052; (408) 721-5000.*

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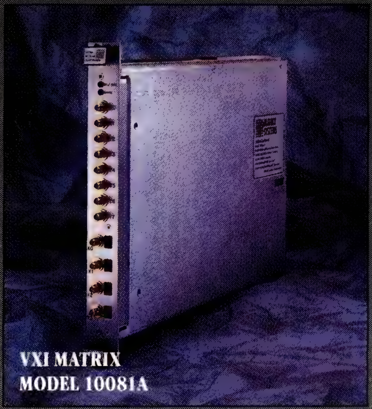

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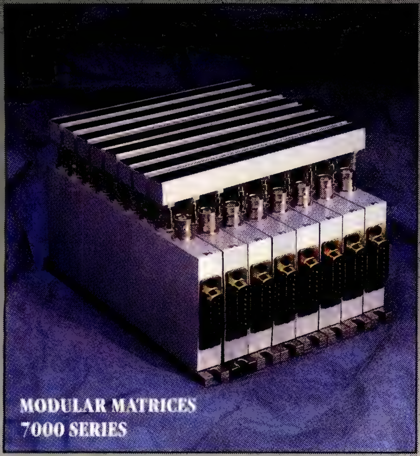

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CIRCLE 143 FOR PRODUCT INFO

# PRODUCTS NEWSLETTER

### REVISED PCMCIA CHIP MEETS MIXED V NEEDS

Following the release of the mixed-voltage physical specification by the Personal Computer Memory Card International Association, designers at Vadem, San Jose, Calif., recharacterized their previously released VG-365 PCMICA and ExCA controller to guarantee compatibility with the mixed-voltage specification (ELECTRONIC DESIGN, June 10, p. 96). The new PCMCIA spec allows for cards that operate at either 5 V or 3.3 V, and future cards that will operate at even lower voltages. The 160-pin VG-365 PCMCIA controller uses external logic buffers to provide either voltage level to the PCMCIA card. The external buffers provide the high-drive output needed to move the signals through long circuit board traces or cables that typically exist on most PCs employing an add-in card/socket for PCMCIA cards. The controller ties directly to either an asynchronous or synchronous ISA bus and includes an activity timer and power sequencing to provide dynamic power management on the cards. Special signals such as SPKR are also supported by the controller, and such signals are passed unmodified to the system bus. In large quantities, the VG-365 costs under $12 each. Call Ahmet Alpdemir, (408) 943-9301. *DB* **CIRCLE 746**

### LOW-VOLTAGE EPROMS PACK UP TO 2 MBITS

Extending its UV EPROM and one-time programmable memory offerings, Advanced Micro Devices, Sunnyvale, Calif., released 3.3-V versions of its 1- and 2-Mbit EPROMs. Designed from the ground up for 3.3-V operation, the chips accommodate systems with unregulated power supplies making it possible for them to operate over a 2.7- to 3.6-V power-supply range. There the Am27LV010 and LV020 families provide 3.0-to-3.6-V operation with capacities of 1 and 2 Mbits, respectively; "B" versions of the same chips provide the extended 2.7-to-3.6-V operating range. The 1-Mbit chips access in as little as 120 ns; the 2-Mbit chips require about 150 ns. Package options include 32-lead ceramic DIPs, LCCs, or a plastic, OTP PLCC. The 1-Mbit chip also comes in a 32-lead thin SOP. In lots of 1000, the Am27LV010-120DC and LV010B-150DC cost $11.15 and $10.35, each, respectively; the LV020-150DC and LV020B-200DC cost $15.00 and $13.55 each, respectively. Call (408) 749-5703. *DB* **CIRCLE 747**

### 6000-GATE FPGAS CLAIM TOP SPEED RATINGS

With a capacity of 6000 gates, the A1460A field-programmable gate array from Actel Corp., Sunnyvale, Calif., allows designers to implement systems with 60-MHz clock speeds. Consequently, the chip can replace subsystems of up to about 60 20-pin high-speed PAL devices and provide up to 168 I/O lines. Tested according to the PREP standard guidelines, the A1460A provides an 11.6-ns clock-to-output, pad-to-pad delay and can implement functions such as a 16-bit loadable counter that can operate at speeds of up to 68 MHz. Even faster versions of the FPGA—possibly 20% to 30% faster—will be available in 1994. The FPGA is the second of the company's ACT 3 family of programmable logic circuits and is supported by the Designer Advantage tool suite, which runs on most popular PC and workstation platforms. The A1460A comes in a 208-lead PQFP and sells for $195 each in lots of 1000. Units are immediately available. Contact Tom Todd, (408) 739-1010. *DB* **CIRCLE 748**

### SPEECH CHIPS TRIM COST, INTELLIGENCE

A trio of speech processors has been added to TSP50Cxx family of synthesizers from Texas Instruments Inc., Dallas, Texas. Combining microprocessor intelligence with linear-predictive coded speech synthesis, the chips make it possible for designers to simplify their systems and lower costs by reducing the chip count. Both the TSP50C04 and C06 include an 8-bit microprocessor that allows designers to combine intelligent functions and speech synthesis without requiring a separate control chip. The chips can hold a maximum of 14 or 28 seconds of speech or high-quality sound effects, respectively. The third chip, the 50C19, includes 32 kbytes of ROM and can hold up to 3 minutes of speech. As with the other new family members, the C19 also includes the 8-bit processor and packs the output d-a converter, some RAM, and various I/O capabilities for system control. These chips are only available in mask-ROM versions and require minimum orders of 50,000 units. In lots of 1 million, the chips sell for $0.85, $1.10, and $2.30 each, respectively, for the C04, C06, and C19. Contact the TI literature center at (800) 477-8924 x3464. *DB* **CIRCLE 749**

*Edited by Clifford Meth*

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# PC-BOARD DELIVERS REAL-TIME COMPRESSION ON 386 PLATFORMS

An add-in video board delivers real-time video compression on both Intel 80386 and 80486-based personal computers at a low price and is fully compatible with the standard decompression codec that's used in Microsoft Video for Windows.

The Pro MovieStudio board from Media Vision Inc. integrates the company's two-chip MotiVE chip set (ELECTRONIC DESIGN, March 4, 1993, p. 37), which is optimized to provide 160-by-120-pixel images at 15 frames/s. The technology does, however, allow users to adjust size and frame rate.

Without the board, a one-minute video file would require 70 Mbytes of storage and eight minutes to complete the compression process in software. The board compresses the file to 4.5 Mbytes in real time. It supports 32,768 colors and can capture resolutions up to 320-by-240 pixels. All major TV standards, including PAL, NTSC, and Secam, are supported and the board has both composite and S-video connectors for interfacing with consumer-level video sources.

Built-in support for the MS Video 1 codec of Video for Windows means that any captured AVI file can be played back on almost any PC platform running Windows with the Microsoft Media Player. Bundled software includes an MS-DOS player and an AVI to Quicktime converter that allows video captured on a PC to be played on an Apple Computer Inc. Macintosh.

The board is available now at a $449 retail price but is also available to OEMs at negotiated pricing.

***Media Vision Inc.**, 3185 Laurelview Ct., Fremont, CA 94538; (800) 348-7116.* **CIRCLE 782**

■ *JACK SHANDLE*

# WORKSTATION FITS ON FACTORY FLOOR

The ZXPC-TFT/WS is an integrated PC-compatible workstation that's designed for machine and process control on the factory floor. The rack-mount industrial workstation features a 10.4-in. full-color TFT LCD and controller, built-in keyboard that retracts when not in use, a 230-W power supply, and four disk-drive bays. The passive backplane supports six full-length PC/AT cards as well as 286-, 386-, or 486-based single-board computers (SBCs). ISA and EISA versions are available. A locking door protects the drives and keyboard and prevents accidental actuation of the reset and power switches. The ZXPC-TFT/WS sells for $6995. The SBCs range from $595 to $3295, with memory costing $70 per Mbyte. RN

***Zendex Inc., 6780A Sierra Ct., Dublin, CA 94568; (510) 828-3000.*** **CIRCLE 783**

# EASE EMBEDDED SYSTEM INTEGRATION

The time-consuming and costly tasks associated with embedded-system integration can be eased using the Computer Tester Analyzer Controller (C-TAC) family of embedded-system support tools. Using the C-TAC, designers can observe the interaction between related subsystems, including LANs, microprocessors, and parallel buses. The data from these subsystems can be time correlated, then processed and stored. The heart of the C-TAC system is the embedded-system profiler, which includes a PC/AT-compatible workstation. The interface between the various subsystems is done across the monitor channel, which can interface to most popular platforms. In addition, custom interfaces are available. The bundled system software offers an intuitive graphical user interface, similar in operation to Microsoft Windows. Prices for the system start at $54,000 and vary depending on configuration. RN

***ITCN, 904 Senate Dr., Centerville, OH 45459; (513) 439-9223.***
**CIRCLE 784**

# 19-IN. X-TERMINAL ADDS SOUND

The MCX line of sound-equipped X terminals now has a new high-end member, the MCX19, which features a 19-in. display and a low-profile base. The 100-Xstone terminal features a 0.28-mm dot pitch and a 72-Hz non-interlaced refresh rate. It offers user selectable resolutions of 640 by 480 to 1152 by 900 pixels. The MCX19 has integrated 16-bit audio I/O support which is network directed. The terminal is built with a 20-MHz MC88100 RISC CPU and supports up to 72 Mbytes of memory. As a result, it can run advanced applications, such as PEX, color imaging, and Display PostScript. Available now, the MCX19 sells for $4695 with 6 Mbytes of RAM. It also includes a mouse, keyboard, serial port, and Ethernet controller. A software license is $50 per unit. RN

***Network Computing Devices Inc., 350 North Bernardo Ave., Mountain View, CA 94043; (415) 694-0650.*** **CIRCLE 785**

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## OPTICAL DRIVE PACKS 128 MBYTES ON 3.5-IN. DISK

With an average seek time of just 28 ms, the LB3128 claims the crown as the fastest 3.5-in. magneto-optical disk drive. Storing up to 128 Mbytes on a 3.5-in. rewritable replaceable platter, the drive supports full MO disks, partial read-only media, read-only media, and fully rewritable media. Developed by LaserByte, the drive complies with the ISO standard for compatibility with 128-Mbyte optical disks and can fit in a standard half-height drive slot. To get the fast seek time, the drive employs a split optical assembly that reduces the weight of the optics that must be mounted on the drive's actuator; as a result, the actuator can move very fast.

Intended for use in high-end personal computers, workstations, and external subsystems for IBM and IBM compatibles, and Apple Computers, the drive is a good match for data-intensive applications such as desktop publishing, multimedia, document imaging, and data archiving. The drive includes a standard SCSI interface that supports SCSI-2 commands. To ensure maximum transfer rates and buffered-write operations, the drive packs a 256-kbyte internal RAM buffer (1 Mbyte optional). Thanks to the buffer, burst transfer rates of up to 4 Mbytes/s are possible, while sustained data rates (limited by the speed of data being read from the disk) of 768 kbytes/s are possible.

Included in the drive are self-testing diagnostics and automatic calibration routines for added reliability. A fast, 3600-rpm spindle motor reduces the latency overhead and maximizes the data rate. The cartridge loading mechanism is rated for a minimum of 10,000 insertion cycles. For OEM evaluation units, expect to spend about $800 apiece, with samples available now. Production will begin in the fourth quarter.

***LaserByte Corp.**, 1330 Bordeaux Dr., Sunnyvale, CA 94089-1005; Stanley Wong, (408) 734-9200.* **CIRCLE 786**

■ DAVE BURSKY

## USE COLOR X-TERMINALS FOR MULTIMEDIA

The Envizex family of color X-terminals comes complete with multimedia capabilities, including CD-quality audio, a local floppy-disk drive, and a scanner interface. The audio input lets users annotate voice-to-text messages. Using the local scanner, documents can be input directly into the Unix operating system. And the floppy drive allows for seamless file transfer between DOS and Unix. The family, which is based on the Intel i960 RISC microprocessor, runs the entire performance gamut, from the 14Ci, a 14-in. display that offers 1024 by 768 pixels and 110,000 Xstones to the 14CaS, a 19-in. display, with 1280-by 1024-pixel resolution and 165,000 Xstones. Prices range from $1995 to $4995. RN

***Hewlett-Packard Co., 300 Apollo Dr., Chelmsford, MA 01824; (800) 637-7740.*** **CIRCLE 787**

## HAND SCANNER HAS NO CONTROLLER BOARD

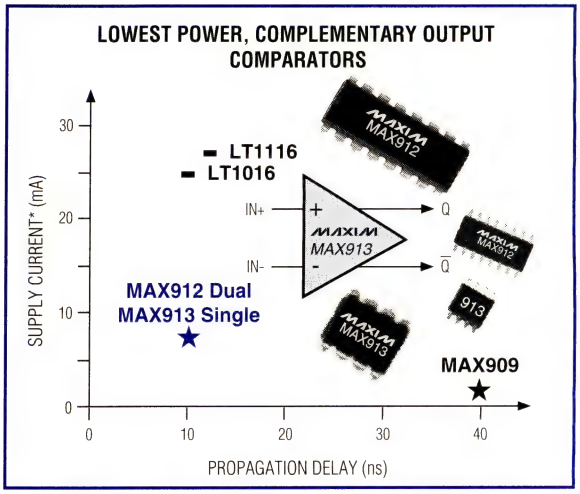
The ScanMan EasyTouch is a Windows-based hand scanner that doesn't require a controller board—it connects to the PC's parallel port. This makes it suitable for portable systems that can't accept controller cards. A pass-through adapter lets the printer operate in the same port without disconnecting the scanner. The scanner's resolution, scan mode, and contrast are software programmable. Bundled software includes an image-editing package and an optical character recognition utility. Minimum system requirements include an IBM-compatible PC with a 386SX processor, 4 Mbytes of RAM, VGA graphics, Windows 3.1, and a mouse. The ScanMan EasyTouch scanner sells for $399. RN

***Logitech Inc., 6505 Kaiser Dr., Fremont, CA 94555; (510) 795-8500.*** **CIRCLE 788**

# 10ns COMPARATORS; 5V TO 10V SINGLE SUPPLY, 70% LESS POWER

## Input Range Includes the Negative Rail, Complementary TTL Outputs

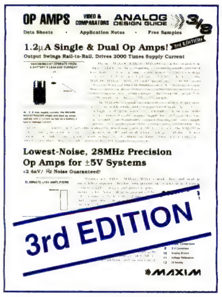
- ♦ 7mA Supply Current per Comparator
- ♦ Single or Dual Supply Operation
- ♦ Latched, Complementary TTL Outputs
- ♦ Inputs Can Exceed Positive Supply without Damage
- ♦ No Power-Supply Current Spiking
- ♦ MAX912–Lowest Power Dual Available
- ♦ Maxim LT1016/LT1116 Also Available



## Select the Lowest-Power, High-Speed Comparators for Your Design

| | | COMPARATORS PER PKG | PROP DELAY (ns) | SUPPLY CURRENT* (mA) | INPUT VOLTAGE RANGE (V+ = 5V, V- = GND) | COMPLEMENTARY OUTPUTS |
|---|---|---|---|---|---|---|
| NEW | **MAX912** | **Dual** | **10** | **7** | **GND to 3.5V** | **YES** |
| NEW | **MAX913** | **Single** | | | | |
| NEW | LT1016 | Single | 10 | 25 | 1.25V to 3.5V | YES |
| NEW | LT1116 | Single | 12 | 27 | GND to 2.5V | YES |
| | MAX901 | Quad | 8 | 2.5 | GND to 2.75V | NO |
| | MAX902 | Dual | | | | |
| | MAX903 | Single | | | | |
| | MAX907 | Dual | 40 | 0.7 | GND to 3.5V | NO |
| | MAX908 | Quad | | | | |
| | MAX909 | Single | 40 | 1.2 | GND to 3.5V | YES |

*Positive Supply Current per Comparator; V+ = 5V, V- = GND.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CIRCLE 186 FOR U.S. RESPONSE CIRCLE 187 FOR RESPONSE OUTSIDE THE U.S.

# THREE CHIP SETS SIMPLIFY THE DESIGN OF SYMMETRICAL MULTIPROCESSOR SYSTEMS WITH UP TO FIVE CPUs

Breaking loose the technology to build 80486-based symmetrical multiprocessor (SMP) systems, Wyse Technologies now offers chip sets, board-level components, and OEM versions of its SMP systems to designers. There are three chip sets: When used together, they allow designers to build SMP systems with up to five CPUs. Such systems could meet or exceed the performance of Wyse's Series 760 SMP, a system that (according to published benchmarks) leads the pack in performance for systems with price tags of between $25,000 and $50,000, and even provides respectable performance when compared with systems that cost ten times as much.

The three chip sets are partitioned according to system function—the Series 700 set, the Series 701 set, and the Series 702 set. The Series 700 set implements a single-CPU EISA-format card while the Series 701 set provides the control logic and buffers for an EISA-format SMP memory card. The Series 702 set supplies all the support logic and buffers to implement a motherboard with multiple EISA and proprietary Wyde-bus expansion slots.

A typical system would thus contain one series 702 chip set, one or more memory boards, each containing a series 701 chip set, and one or more CPU cards, each containing a series 700 chip set.

Of the five chips in the series 700, one handles the cache control and another performs bus control. Two more provide the data-path buffers, and the fifth buffers the address path.

In the 701 chip set, one chip controls all the addressing and four chips buffer the address bus. Five chips buffer the 128-bit wide data bus.

In the 702 chip set, one chip is a system controller and another performs bus control. The rest of hte chips are buffers for the Wyde memory-bus and Wyde data-bus interface.

Wyse has also developed Verilog simulation models of all the chips and buses to aid in the system development stage. Such models are only available to serious customers committed to an SMP system design.

A kit of all chips and supporting documentation sells for $800. Each additional CPU chip set adds $299. Pre-assembled boards or cages are also available. Software for the hardware adaption layer to interface the hardware with Microsoft's Windows NT or Sun's Solaris operating systems, and support from Phoenix for BIOS development, is also available.

***Wyse Technology Inc.**, 3471 N. First Street, San Jose, CA 95134-1803; Jack Kister, (408) 473-1200.* CIRCLE 789

■ *DAVE BURSKY*

# ICs FOR WORKSTATIONS PROVIDE 3:1 DATA COMPRESSION AT REAL-TIME DATA RATES OF UP TO 40 MBYTES/S

Although data-compression utilities have been available for PCs and Apple Macintosh computers for a number of years, the higher-performance workstations and larger systems have had to run without compression. Performing real-time compression with previously-available silicon solutions would have slowed the systems to unacceptable performance levels.

But that scenario now changes with the release of high-performance lossless compression engines and ASIC building blocks from IBM. The circuits are based on the widely used Lempel-Ziv algorithm and can compress data by an average of 3:1 at speeds that make the operation transparent to the host system—up to 40 Mbytes/s.

The two initial offerings include the ALDC1-5S and the ALDC macro. The former is a chip that runs at a rate of 5 Mbytes/s. The ALDC macro, an ASIC core, can run rates of up to 40 Mbytes/s.

The stand-alone chip version can compress or decompress data at rates of up to 5 Mbytes/s (in each direction). It includes a 512-byte history buffer on the chip.

The embedded buffer eliminates the need for an off-chip memory, making the ALDC1-5S a one-chip solution. Designed for incorporation directly in the I/O channel, the chip can transparently compress and decompress data being transferred between a peripheral and the host system. The small-format package—a 100-lead thin PQFP—easily lets the chip fit on anything from a PCMCIA card to a system motherboard.

By placing the adaptive lossless data-compression circuit in the I/O path rather than as a bus peripheral, system performance can be maintained without any impact on the operating system. Consequently, such a solution is aimed at new designs rather than as an upgrade to existing systems. However, the incorporation of data compression in a peripheral such as a multidrive storage subsystem could not only double to triple the storage capacity, but also improve data transfer speeds. The speed increase is potentially possible since compressed data would appear to be read or written two- to three-times faster than uncompressed data.

Samples of the stand-alone ADLC1-5S chip will sell for between $20 and $30 each, while the ALDC macrocell, which measures just a few millimeters on a side, is immediately usable and is included as part of IBM's ASIC library.

***IBM Corp.**, 1000 River Street, Dept. N97/Bldg. 861-2, Essex Junction, VT 05452-4299; Ted Lattrell, (802) 769-6408.*

CIRCLE 790

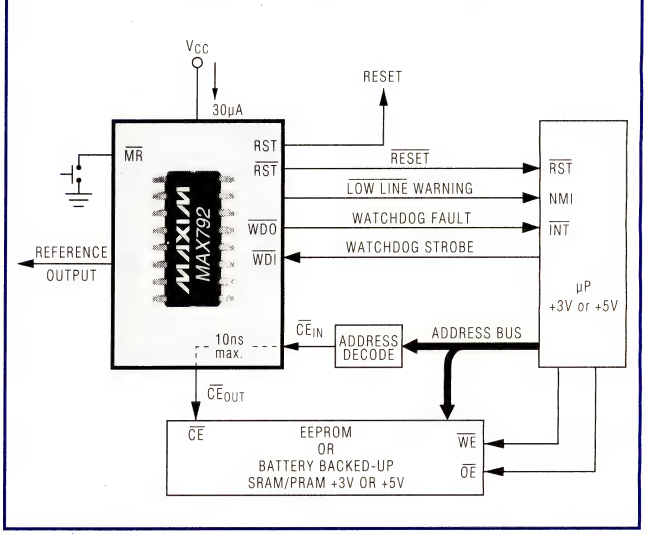
■ *DAVE BURSKY*

# 6-FUNCTION µP SUPERVISOR PREVENTS FALSE WRITES TO 3V & 5V MEMORY

The MAX792 has the shortest chip-enable delay (10ns) available in a µP supervisor. During power failures, the supervisor prevents unwanted memory-write operations. The MAX792 also provides reset, watchdog, low-line, overvoltage-detection, and manual-reset functions. The MAX792 is optimized for 3V or 5V systems that do not require battery switchover circuitry. If switchover is needed, please refer to the µP Supervisory Design Guide: over 44 different devices are available.

- **3V & 5V Versions**
- **10ns max Chip-Enable Gate Delay**
- **Memory Write-Cycle Completion**
- **$\overline{\text{RESET}}$ and RESET Outputs**
- **Five Trip Thresholds for Reset**
  **4.62V, 4.37V, 3.06V, 2.91V, 2.61V**
- **Adjustable Trip Threshold for Reset**
- **Low Supply-Voltage Warning**
- **Adjustable Watchdog-Timeout Delay**
- **Overvoltage Warning**
- **Manual-Reset Input**
- **140ms min. Reset-Timeout Delay**
- **Guaranteed $\overline{\text{RESET}}$ Valid to $V_{CC}$ = 1V**
- **Low 30µA Operating Current**
- **Space-Saving 16-Pin Narrow SOIC**

**ECONOMICAL 3V, 3.3V OR 5V FALSE-WRITE PROTECTION**



*The MAX792 is the only µP Supervisor available that provides chip-enable gating for 3V and 3.3V systems. The 5V versions provide protection for EEPROM and other nonvolatile memories.*

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# ENHANCED DSP IC IS AIMED AT DIGITAL CELLULAR COMMUNICATIONS

Designed to handle voice compression, modem, and control functions for next-generation digital cellular communication systems in the U. S. and Japan, the DSP56166 runs at an internal clock speed of 60 MHz, which lets it execute up to 30 MIPS. The chip combines the 16-bit high-speed 56100-family digital signal processor core, a sigma-delta codec, a phase-locked loop (PLL), and Motorola's on-chip emulation (OnCE) capability. The single-chip DSP/codec can serve as a single-chip voice processor for a wide range of communication applications.

Like the earlier DSP56156, the DSP56166 has a 14-bit codec and clock-multiplying phase-locked loop. However, the on-chip memory has been enhanced to include a 4-kword-by-16-bit data RAM, a 256-by-16 program RAM, a 4-k-by-16 data ROM, and an 8-k-by-16 program ROM. The on-chip phase-locked loop lets the chip accept input clock frequencies from 15 kHz up to the full speed of 60 MHz, and deliver full performance at any input frequency. An output clock synchronized to the synthesized internal clock also helps improve the synchronous timing of the chip's external memory port.

The 56166 has external 16-bit address and data buses to supply access to 64 kwords each of program and data RAM. There are also 25 general-purpose I/O pins; two, independent, reduced synchronous serial interfaces; and one 16-bit timer. The OnCE port allows simple, speed-independent access to all internal registers and memory, as well as access to external memory. Designers can get the status of all the registers, memory locations, buses, and even the last five instructions executed. When housed in a 112-lead PQFP, the DSP56166 sells for $60 a piece in thousands. Samples are available now.

***Motorola Inc.,*** *DSP Div., 6501 William Cannon Drive W, Austin, TX 78735-8598; (512) 891-2030.* CIRCLE 791

■ *DAVE BURSKY*

# GRAPHICS SUPPORT CHIP RESIZES VIDEO IMAGES AND PUTS THEM IN A WINDOW

Able to accept NTSC video from a camcorder, a TV tuner, as well as full-motion digital video, the PC View chip can resize the image and display it in a window. Developed by Trident Microsystems, the chip supports Microsoft's Video for Windows, as well as JPEG, MPEG, Indeo, DVI, CD ROM-I, and CD ROM-XA encoded data to provide low-cost video on desktop and portable computers.

In addition to handling the live or digitized video and resizing the image via a line-dropping algorithm, the PC View processor lets users perform frame capture, linear zooms (1 to 16X), pans, mosaics, and even do chroma keying to the VGA or video source for overlays. To trim system cost, the chip can use low-cost DRAMs instead of more expensive video RAMs. The PC View chip also needs only 512 kbytes of DRAM, rather than the 768 kbytes of VRAM typically used by other adapters.

To trim the memory requirements, Trident designers crafted a more efficient and proprietary hardware color compression algorithm that halves memory requirements. A color-space converter block is also included on the chip to support YUV and RGB signals, letting the chip tie directly to JPEG and MPEG compression subsystems. The RGB support allows the use of 8-bit RAMDACs, permitting low-cost system designs.

The PC View chip handles memory control, bus interface timing, and CRTC control. It can overlay video on 16-bit VGA at 640-by-480-pixel resolution or the VGA in the frame buffer can be overlayed onto the video, thus permitting titles and graphics to be added. An $I^2C$ interface on the chip allows the circuit to communicate with various peripheral support functions. In lots of 1000, the PC View sells for $30 each. Samples as well as a reference board design are immediately available.

***Trident Microsystems Inc.,*** *205 Ravendale Drive, Mountain View, CA 94043; Mike Maia, (415) 691-9211.* CIRCLE 792

■ *DAVE BURSKY*

# FLEXIBLE FLASH MEMORY MODULE PACKS 4 MBITS

Configurable as 128 kwords by 32 bits, 256 kwords by 16 bits, or 512 kwords by 8 bits, the WF-128K32-XHX 4-Mbit flash memory module comes with access times of 120, 150, or 200 ns. The hermetically sealed 1.18-in.$^2$ module is less than 0.25-in. high and is built around a multilayer ceramic substrate with 66 pins arranged in a pin-grid-array hex-in-line layout. For reads, the module requires 5 V, while to write to or erase the memory, 12 V dc is needed.

Data storage operations require 10 µs/word, and a minimum of 10,000 erase/program cycles are guaranteed. On standby, the module draws just 8 mA, while peak operating current is 150 mA for the by-32 configuration, 80 mA for the by-16, and 40 mA for the by-8 version. The module comes in three operating-temperature-range options—0 to 70, -40 to +85, and -55 to +125°C. Small quantities are available from stock to four weeks with OEM prices starting at $800. DB

***White Technology Inc., 4246 E. Wood Street, Phoenix, AZ 85040; Jack Bogdanski, (602) 437-1520.*** CIRCLE 793

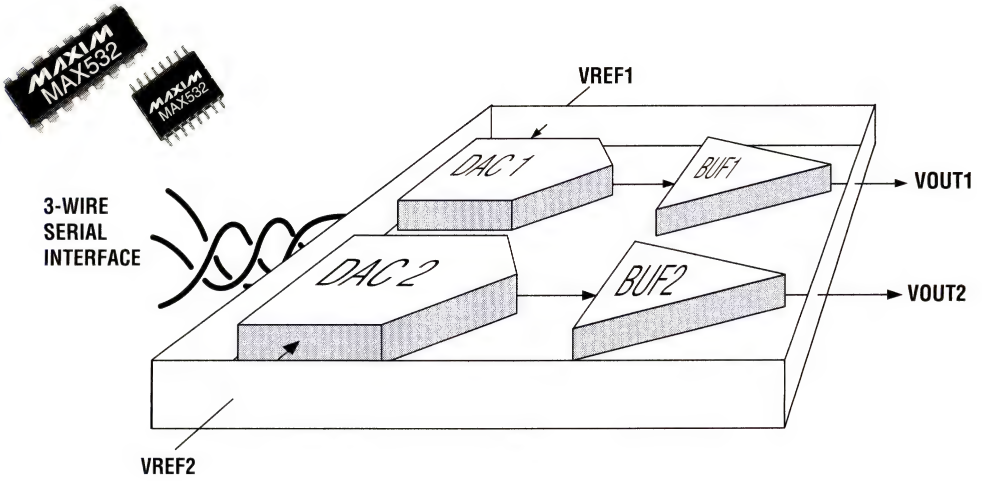
**Correction**

The price for the Keycoders product from USAR Systems (New York, N.Y.), mentioned in our Sept. 2 issue (p. 150) should be $9.12 ea. in lots of 1000, not $9.00 ea. in lots of 10,000.

# DUAL SERIAL 12-BIT DAC CUTS SPACE & COST 35%

The new MAX532 combines two precision, voltage-output 12-bit DACs in a 16-pin DIP or SOIC package. A fast 3-wire serial interface simplifies signal routing and opto-isolation – and frees microprocessor pins. And at $8.45, the MAX532 costs at least 35% less than space-consuming alternatives.

## Two Voltage-Output 12-Bit DACs in 16-Pin DIP/SO – $8.45†



- ◆ **Fast 6MHz Serial Interface**
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- ◆ **±12V Output Swing**
- ◆ **±10mA Output Current**
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† 1000-up Recommended Resale, FOB, USA

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**CIRCLE 206 FOR U.S. RESPONSE** **CIRCLE 207 FOR RESPONSE OUTSIDE THE U.S.**

# VECTOR GENERATOR MIMIMIZES TEST PROGRAM GENERATION

A test vector-generator technology called the Safecracker Algorithmic Vector Generator creates high-fault-coverage, pin-level test patterns in hours using only rudimentary data about the device pins and no information about the device's function. The technology allows users to generate board-level in-circuit test patterns for non-boundary scan digital devices that lack test patterns or model libraries or which would require too much time, skill, or expense to produce patterns manually.

The Safecracker software uses sophisticated goal-seeking and vector minimization techniques to create patterns that detect digital solder open and stuck-at pin faults for static VLSI and custom devices such as ASICs, PLDs, and FPGAs. Vectors are created by interfacing a sample device to a device stimulus-measurement unit (containing controller and channel cards), a device adapter, and DOS-based software. The operator defines the purpose of each pin (input, output, bidirectional, etc.) and sets goals that the test vector must satisfy. To give Safecracker a "head start," the operator can suggest goals, starting vector sets, or clock and bus events. While the system is running the operator can interact with Safecracker to suggest, modify, and delete goals to avoid unproductive loops.

The Safecracker capability is offered through the Safecracker Pattern Service. Price depends on the number of pins and requested turnaround time. Patterns for a typical 80- to 100-pin ASIC will cost about $1000 for a 10-day turnaround. Safecracker will also be sold as a standalone system for about $50,000, with delivery in 90 to 120 days. Initial licenses will be for Z1800VP-series testers only, but other licenses will be offered in the future.

***Teradyne Inc.,** 321 Harrison Ave., MS L-57, Boston, MA 02118; (617) 422-3567.* CIRCLE 794

■ *JOHN NOVELLINO*

# LOGIC ANALYZERS GET FULL PENTIUM SUPPORT

Full Pentium microprocessor support is now available on the GPX general-purpose logic analyzer and the DAS 9200 systems analysis platform. The support includes a probe adapter and full disassembly capability at speed (66 MHz). The capability includes the identification and labeling of non-executed instructions, even with speculative prefetching; comprehensive real-time trace; sophisticated performance analysis; and 10-ns triggering. The GPX Pentium support costs $4000, but is free to those who buy a two-module GPX system by Nov. 26. The DAS support costs $6000, but is free to anyone who buys certain DAS upgrades before Nov. 26. Delivery is in 6 weeks. JN

***Tektronix Inc., Test and Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200.*** CIRCLE 795

# SOFTWARE MODULE DOES STATISTICAL OPERATIONS

As an add-on module to the DADiSP graphical data analysis software, DADiSP/Stats allows users to perform a comprehensive set of statistical tests and present statistical information graphically. The menu-driven module generates a presentation-quality text report or graphical result that can be incorporated into a document or sent directly to a printer. Some of the operations possible include descriptive statistics, column and row statistics, correlations, graphical fit, and polynomial curve fitting. The menu and macro files are ASCII (readable) files, so users can view the functions and menus to verify the algorithms or modify the functions and menus. DADiSP/Stats costs $495 for PCs and $795 for workstations. JN

***DSP Development Corp., 1 Kendall Sq., Cambridge, MA 02139; (617) 577-1133*** CIRCLE 796

# I/O BOARDS, SOFTWARE CREATE TOTAL SOLUTION

DataAcq-EZ offers a low-cost solution for Windows-based data acquisition. Three analog and digital I/O boards are available. The DT01-EZ supplies 12-bit resolution and 27.5-kHz throughput. The DT21-EZ offers 12-bit resolution with 50-kHz throughput, and the DT16-EZ provides 16-bit resolution with 7.5-kHz throughput. Each board has two independent digital-to-analog converters and two 8-line digital I/O ports. The STP-EZ screw terminal panel with cable assembly allows easy hook-up the boards' I/O lines. The boards are supported by VB-EZ, which transforms Visual Basic into a complete data-acquisition package, including fast plotting for real-time analysis. The DT01-EZ costs $595, the DT21-EZ $795, and the DT16-EZ $995. VB-EZ costs $195, and the STP-EZ costs $99. Delivery is within five days. JN

***Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752-1192; (508) 481-3700*** CIRCLE 797

# EMULATOR SUPPORTS 68360 COMM CONTROLLER

Full emulator support is now available for the Motorola 68360 Quad Integrated Communications Controller. The EL 3200 for the 68360 features Ethernet capability, 4-Mbyte/min. code downloading, intelligent trace disassembly, statistical performance analysis, and a sophisticated event breakpoint system. Debugging features include extended source-level debugging using XICE, a windowed interface that supports tool chains from several manufacturers and offers the choice of working at the source-code, symbolic, or assembly-language level. A complete EL 3200 for the 68360 costs about $25,000. Delivery is in 4 to 6 weeks. Users who own a chassis for the 68330/340 can upgrade to the 68360 for about $14,000. JN

***Applied Microsystems Corp., 5020 148th Ave. N.E., Redmond, WA 98073-9702; (206) 882-2000.*** CIRCLE 798

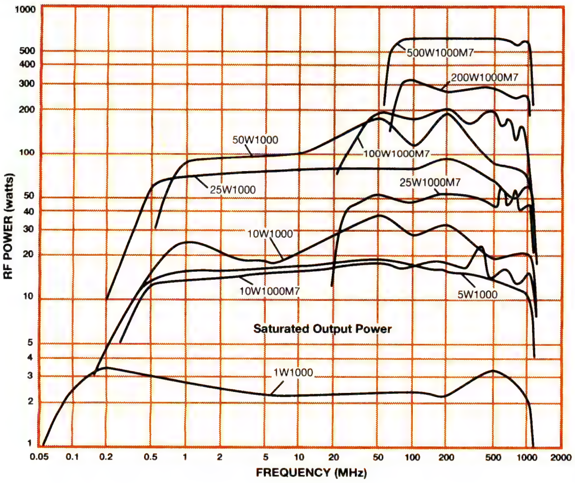
# When it gets lonely out there at 1 GHz, you'll be glad you have all this power.

The only amplifier that can deliver 500 watts through that balky decade from 100 to 1,000 MHz is our new Model 500W1000M7. That's the majestic one on the left, with the front-panel bi-directional power meter, ALC, and a bagful of other controls that will let you actually *enjoy* automatic sweep testing in your lab.

The 500W1000M7 presently heads our well-known "W" Series of all-solid-state linear amplifiers that cover four crucial decades of bandwidth from 100 kHz to 1 GHz. Today, you may need only 1 watt (the little portable on the top), or 5, or 10, or 25, or 50, or even 100 or 200 watts *minimum*—all with that fantastic bandwidth instantly available without tuning or bandswitching—a combination of power and bandwidth that's comforting when you work the outer reaches of the rf spectrum. Wherever your power requirements are today, they're sure to go up. And one of these days you're going to want a 500W1000M7.

The "W" Series is part of a complete line of AR amplifiers offering rf power up to 10 kilowatts for rf susceptibility testing, nmr spectroscopy, plasma/fusion research, and a host of other test situations that demand rf power of unconditional stability—immunity to even the worst-case load mismatch, shorted or open cable, wild swings of VSWR—with no fear of oscillation, foldback, or system shutdown.

You might learn a lot from our free booklet, "Guide to Broadband Power Amplifiers." Send for a copy. Or call our toll-free number (800-933-8181), which will connect you directly to one of our applications engineers.



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**TEL 215-723-8181 • FAX 215-723-5688**

*For engineering assistance, sales, and service throughout Europe, call* EMV: Munich, 89-612-8054 • London, 908-566-556 • Paris, 1-64-61-63-29

**CIRCLE 144**

5351

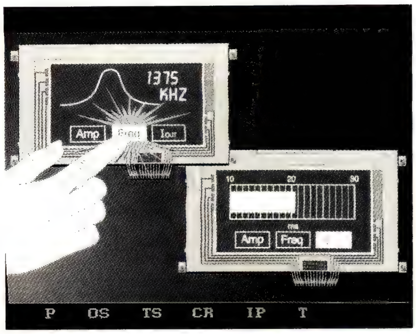
## LEADLESS SMT DIODE MATCHES 0805 OUTLINE

The BAS216 general-purpose switching diode is claimed as the first to be housed in a ceramic SMT package with exactly the same pc-board footprint as an 0805 chip capacitor. The device is housed in Philips's SOD110 ceramic package and meets the small-signal-diode switching characteristics found in most circuits. Repetitive peak forward current and continuous dc forward current ratings are 500 mA and 250 mA, respectively. The units repetitive peak reverse voltage spec is 85 V and its maximum reverse-recovery time is 6 ns. Call for pricing and delivery information. DM

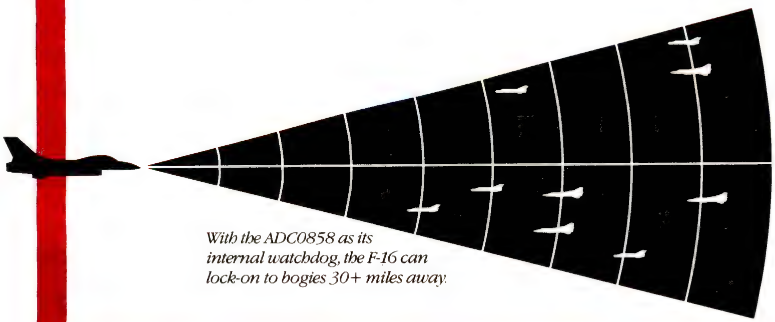
***Philips Components, Discrete Products Div., P.O. Box 10330, Riviera Beach, FL 33404; (800) 447-3762.*** **CIRCLE 799**

## TOUCH-PANEL LCD GRANTS FLEXIBILITY

A dot-matrix touch-panel LCD features either 256-by-64- or 256-by-128-pixel display resolution and supertwisted nematic display technology to offer a state-of-the-art user interface. With the panels, users can create their own character and graphics screens, buttons, labels, and custom fonts. The complete touch-panel module measure just 16 mm thick and incorporate a highly transparent film-and-glass panel that's both durable and reliable. The display, with its single- or dual-CFL (cold-cathode fluorescent lamp) backlighting, is bright and uniform even at its periphery. Efficient circuit design has reduced LCD power requirementsw to a single +5-V supply. Pricing in lots of 100 is $138.54 for the 256-by-64-pixel model and $185.71 for the 256-by-128-pixel display. Delivery is from distributor stock. DM



***II Stanley Co. Inc., 2660 Barranca Pkwy., Irvine, CA 92714; Bill Roth, (800) LED-LCD-1.*** **CIRCLE 800**



MIL/AERO UPGRADE #7

With the ADC0858 as its internal watchdog, the F-16 can lock-on to bogies 30+ miles away.

8-Bit Analog-to-Digital Converter

THIS WATCHDOG™ MONITOR keeps all analog functions in check. Our new 8-bit ADC delivers flight-critical monitoring of temperature, voltage and current. As a result, your µP is free to do other vital tasks and you're guaranteed 100% system operation. What's more, the ADC0858 features programmable limits, an on-board MUX, eight analog inputs, +5V operation and a mere 50mW power budget. For a free sample, here's *your* number: 1-800-NAT-SEMI, Ext. 249.

MIL STD ★COMPLIANT★ 883

Here today. Backed tomorrow.

National Semiconductor

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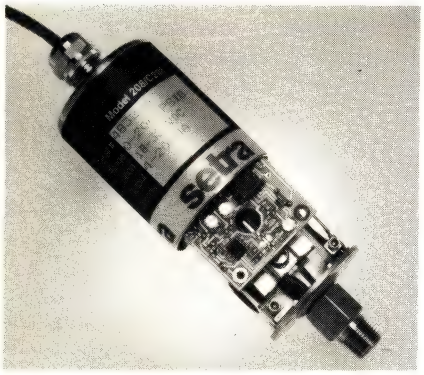
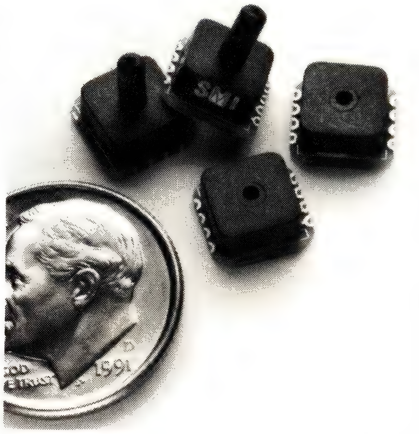
## PRESSURE TRANSDUCERS OFFER HIGH STABILITY



Accuracy that's maintained even during extremes of mechanical shock and vibration, thermal shock, RFI, and corrosive media is featured in the C-208 gage pressure transducer. The unit holds its accuracy of ±0.25% of full scale, hysteresis of only 0.1% of full scale, and stability of 0.5%/year. Available in pressure ranges of zero to 50 and zero to 5000 psig, the C-208 transducer uses a rugged squeeze-tube sensing element that eliminates reliability problems associated with strain gages, semiconductors, and other measurement techniques. Call for pricing and delivery. DM

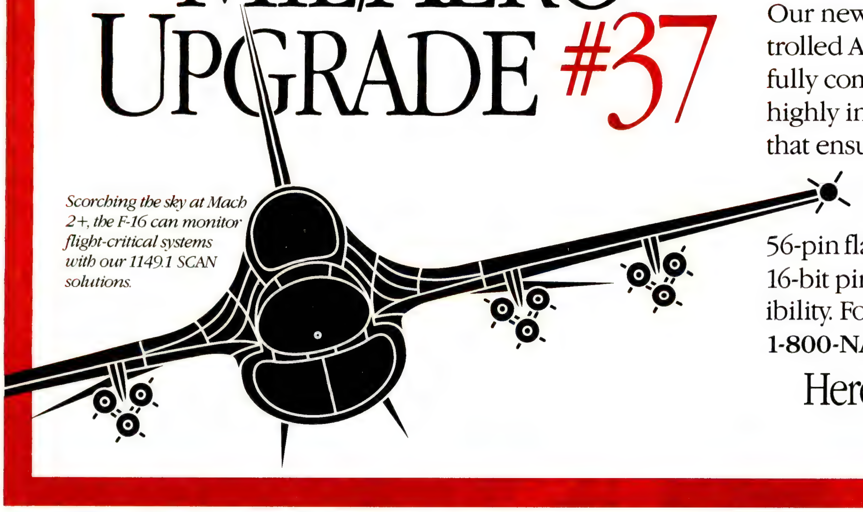
***Setra Systems Inc., 45 Nagog Park, Acton, MA 01720; Todd Martin, (800) 25-SETRA.*** **CIRCLE 801**

## SMT PRESSURE SENSORS BOAST STABILITY GAINS



A low-cost line of surface-mounted pressure sensors uses a newly designed piezo-resistive, micromachined silicon chip that improves on the stability and long-term drift characteristics of traditional silicon structures. The 5300 Series sensors are offered in 5-, 15-, 30-, 60-, and 100-psi full-scale pressure ranges. With their 0.3-by-0.3-in. footprint, the sensors are well-suited for high-volume applications using automated assembly. The chips are mounted on an epoxy-glass substrate, which offers the advantage of a closer match to the CTE of silicon than the usual ceramic substrate. Call for pricing and delivery. DM

***Silicon Microstructures Inc., 46725 Fremont Blvd., Fremont, CA 94538; Steve Repetto, (510) 490-5010.*** **CIRCLE 802**



MIL/AERO UPGRADE #37

*Scorching the sky at Mach 2+, the F-16 can monitor flight-critical systems with our 1149.1 SCAN solutions.*

SCAN Solutions (1149.1)

BOUNDARY SCAN TESTING has never been easier. Our new family of 18-bit SCAN™ (Serially Controlled Access Network) solutions are fully compliant to IEEE 1149.1. It's a highly integrated, low-power family that ensures radiation tolerance, high drive and low noise. SCAN solutions come in 56-pin flatpaks—extensions of JEDEC's 16-bit pinout to maximize future upgrade flexibility. For a free sample, here's *your* number: **1-800-NAT-SEMI, Ext. 249.**

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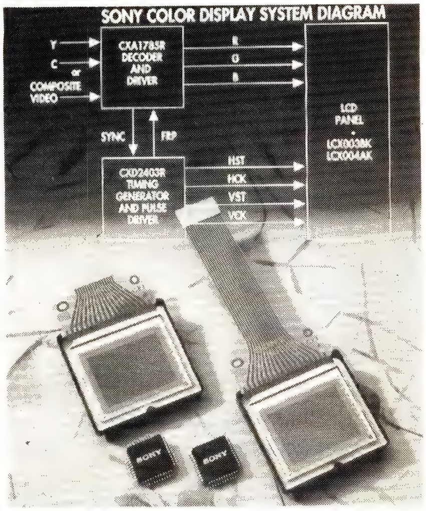
## 0.7-IN. COLOR LCDS TARGET VIEWER TASKS


SONY COLOR DISPLAY SYSTEM DIAGRAM
Y
C
or
COMPOSITE VIDEO
CXA1785R DECODER AND DRIVER
R
G
B
SYNC
FRP
CXD2403R TIMING GENERATOR AND PULSE DRIVER
HST
HCK
VST
VCK
LCD PANEL
LCX003BK
LCX004AK
SONY
SONY

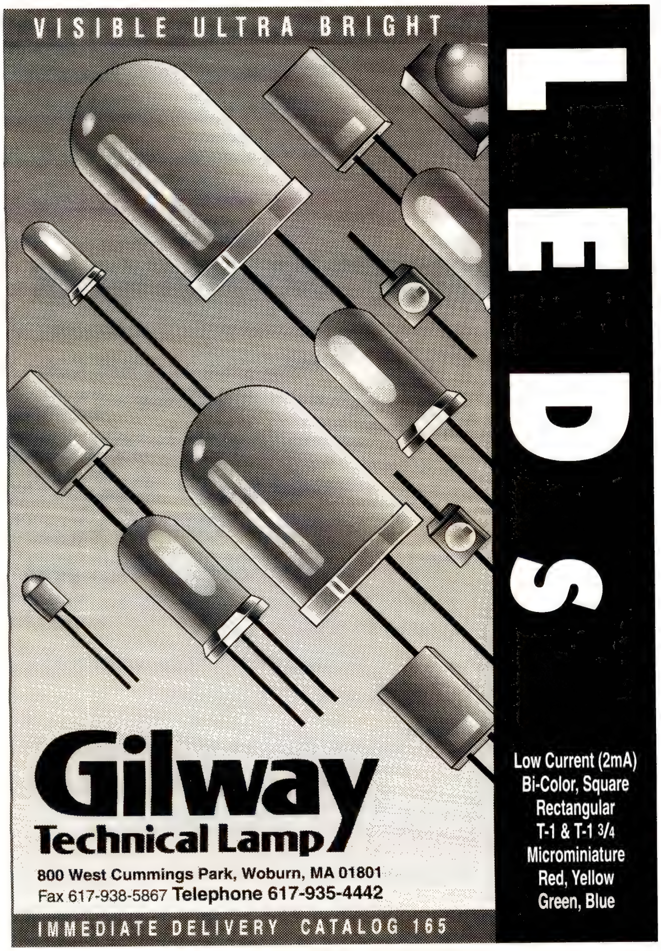
NTSC and PAL versions of 0.7-in.-diagonal color-LCD panels are available with their associated decoder/driver and timing-generator/pulse-driver ICs. The LCX003BK and LCX004AK panels are active-matrix panels designed for use with NTSC and PAL video signals, respectively. The LCX003BK panel has a pixel density of 103,114 while the LCX004AK has a density of 122,980 effective pixels. The outline dimension of each panel is 22 by 21 mm with an active display area of 14.2 by 10.7 mm. Two associated ICs form a complete color panel system when used with the display panels. The CXA1785R decoder and driver converts composite video signals into RGB signals for the panels. The CXD2403R is a timing generator for driving the LCDs. Sample pricing for the LCX003BK and LCX004AK display panels is $167 and $175, respectively. The CXD2403R timing-generator IC goes for $8.35 and the CXA1785R decoder/driver IC costs $7.92. DM

*Sony Electronics Inc., Component Products Co., P.O. Box 6016, Cypress, CA 90630-0016; (800) 288-SONY.* **CIRCLE 803**

## 500-W SUPPRESSOR GUARDS 12 LINES

Protection of combinations of eight or 12 unidirectional or bidirectional data lines is achieved with the DA Series 500-W diode-array transient-voltage suppressors. The devices are designed for board-level protection of standard TTL or MOS bus lines in applications where static electricity or other voltage surges can damage or upset voltage-sensitive circuitry. Features include high surge capability, extremely fast response time, low on-state impedance, and applicability to ac and dc circuits. Pricing in lots of 1000 starts at $2.20. Delivery of OEM quantities takes from eight to 14 weeks from receipt of order. Sample quantities are delivered from stock. DM

*ProTek Devices, P.O. Box 3129, Tempe, AZ 85280-3129; Richard von Barandy, (602) 968-6060.* **CIRCLE 804**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CIRCLE 94 FOR U.S. RESPONSE
CIRCLE 95 FOR RESPONSE OUTSIDE THE U.S.

SIMULATION DATA MANAGEMENT

SOURCE III provides a suite of CAE tools for dealing with the generation, translation, verification and analysis of logic simulation data files. The software is available on most workstation platforms and interfaces to over 25 popular logic simulators.

VGEN® — VECTOR GENERATION

**VGEN** is a high-level, simulator-independent Stimulus Generation language that makes it easy to create, modify, document and maintain simulation stimulus files. **VGEN** can reduce stimulus development time by up to 80% and provides a common front-end to most logic simulators.

VTRAN® / VTEST™ — VECTOR TRANSLATION

**VTRAN** is a vector translator which provides a vital link between the many dissimilar logic simulation data formats in use today. **VTRAN** solves the data translation problems inherent in applying multiple simulation and verification tools to a design project. **VTEST** works with **VTRAN** to create functional test programs for device testers from simulation results data.

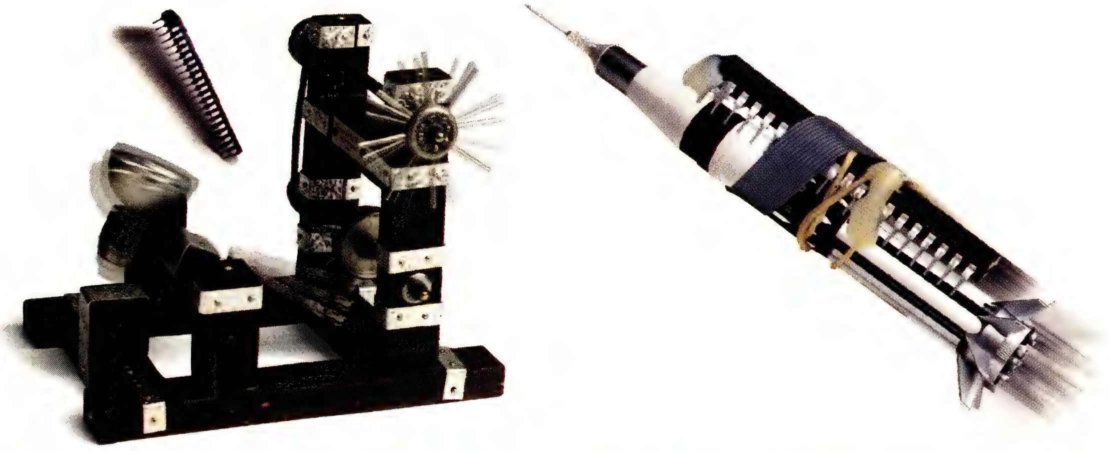
VCAP™ — VECTOR COMPARISON/ANALYSIS

**VCAP** is a comprehensive comparison and analysis program which automates the verification of simulation results against expected results, results from previous runs, or results from different simulators.

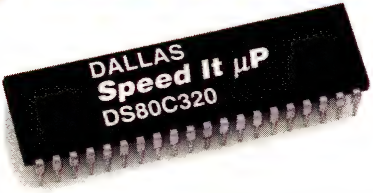
*Call or write for information:*
SOURCE III, Inc.
3958 Cambridge Road, Suite #247
Cameron Park, CA 95682
(916) 676-9329

CIRCLE 120 FOR U.S. RESPONSE
CIRCLE 121 FOR RESPONSE OUTSIDE THE U.S.

# Running out of tricks to make the 8051 go faster?



# Try the only 8051 built for speed.



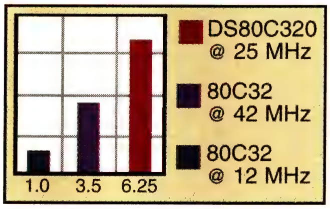
Since its introduction a short time after the dark ages, the 8051 hasn't really improved. Until now. The DS80C320 High-Speed Micro runs up to three times faster than other 8051s using the same crystal.

## Fewer Clocks for Greater Performance

We redesigned and updated the architecture using four clocks per instruction instead of the usual 12. You needn't be a math whiz to figure out that when the same instruction takes 1/3 the clocks, software can do more in less time.

## Drop In For Speed

The DS80C320 is a drop-in replacement for 80C31- or 80C32-based designs. So you can plug it into your system with no redesign and get an instant performance improvement, regardless of the speed at which your system runs. With an adjustable speed interface to RAM and peripherals, the DS80C320 is easy to adapt to existing hardware.



*The DS80C320 outperforms other 8051s even when they use higher clock speeds. A DS80C320 running up to 25 MHz can do almost twice as much work as a standard 8051 running at over 42 MHz.*

At its top speed of 25MHz, the DS80C320 performs an instruction cycle in 160 ns. And you can look for higher speeds from Dallas soon.

## Long-Awaited Improvements

But speed isn't the only improvement we've made. For example, we've added a Dual Data Pointer. A second, full-function UART that is completely independent from the original. Six external interrupts instead of the usual two. A power monitor that provides early-warning interrupt and power-fail reset. Even a programmable watchdog timer.

The DS80C320 offers all these features, with no external components, in the standard pinout. It's still fully 8051 instruction set-compatible and offers the familiar 256 bytes of RAM and three 16-bit timers.

To see what the **8051 for the 90s** can do for your design, give us a call.

**DALLAS**
**SEMICONDUCTOR**

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CIRCLE 148 FOR U.S. RESPONSE CIRCLE 149 FOR RESPONSE OUTSIDE THE U.S.

# REAL-TIME CASE TOOLS PORTED TO SUN

Now that a suite of real-time CASE tools has been ported from Unix to Solaris 2.x/Sparc, users of Sun workstations have another option among 32-bit tools for developing mission-critical applications. The software engineering tools for Solaris 2.x include Logiscope, LOV, Geode, Adele, and ASA. Logiscope is aimed at software quality analysis, test, and maintenance. Logiscope processes 60 different languages and dialects, including C, C++, Ada, Cobol, Fortran, and Pascal. Dedicated to object-oriented development, LOV supports developing large-scale software and creating and managing reusable components.

Geode, intended for real-time design, uses the graphical, formal Specification and Description Language (SDL), to model the properties of complex systems. Adele is an advanced configuration-management system, supplying data integrity in large systems, support of process management, customization, and a choice of interfaces.

ASA, a set of tools for requirements analysis and system validation, allows users to create an executable model of the system. ASA also supplies automatic production of test scenarios for system acceptance test regarding descriptions, verification, and automated test generation. Logiscope goes for $16,000 to $20,000 per computer, depending on configuration. LOV is available now. Geode and Adele ship this month. ASA will be available in December. Pricing for LOV, Geode, Adele, and ASA will be announced upon shipment.

***Verilog**, 3010 LBJ Fwy, Suite 900, Dallas, TX 75234; (214) 241-6595; fax -6594.* **CIRCLE 805**

■ *SHERRIE VAN TYLE*

# NT X-SERVER SOFTWARE AIMS AT R4000

Targeting Mips Technologies' R4000 RISC processors, XoftWare/32 for Windows NT adds 32-bit X11R5 server capabilities to MIPS-based PCs using the Microsoft Windows NT operating system. The software enables users to concurrently access and display Windows, NT and Unix-based applications on the same PC. It automates host login and application start-up through an icon-based click & start feature. A multiprocess startup system enables multiple applications to start simultaneously. Production shipments of XoftWare/32 for Windows NT will begin after Microsoft's official shipment of NT. List price is $495, with multiple package discounts and site licenses. SVT

***AGE Logic Inc., 9985 Pacific Heights Blvd., San Diego, CA 92121; (619) 455-8600; fax (619) 597-6030.*** **CIRCLE 806**

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Conner Drives Right Past Colorado.

| Feature | Conner Tape•Stor 250 MQT w/Backup Basics Software | Conner Tape•Stor 250 MQT Plus w/Backup Exec Software | Colorado DJ-20 |
|---|---|---|---|
| Drive Size | 1" Industry Standard | 1" Industry Standard | NO |
| Free 3M Tape | YES | YES | NO |
| DOS/Windows Software | YES | YES | NO |
| 2-Year Warranty | YES | YES | NO |
| Full Cartridge Insertion | YES | YES | NO |
| Suggested Retail Price | $179.99, with all the above, including a formatted 3M minicartridge | $199.99, with all the above, including a formatted 3M minicartridge | $199.99 |

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The Storage Answer

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## i960 TARGET BOARDS GET INTERFACE SUPPORT

Intended for use with the Ada/i960MM/MX software development environment, the Custom Target Board Interface Kit software package gives a system designer a simplified interface between the designer's i960 target board and the company's Ada/i960MM/MX software development environment.

The interface kit includes a micro-debugging kernel, communication driver, task scheduling, and memory-management features. The interface kit is the first such product available for Intel's i960MM/MX microprocessor, the company says.

The interface kit controls the interface between the i960 development environment and the user's i960-based target board at the Ada runtime, at the source-level debugger, and at the communication link between the host and target. With the board interface kit, the system design controls the operation of the Ada runtime environment on the target board by means of the micro-debugging kernel.

The kernel also controls all task scheduling and memory management features, besides controlling the interface between the source-level debugger and the target board. The debugger supports breakpoint and watch point conditions and enables the user to evaluate Ada expressions with symbol overloading or qualification.

The kit supports host-to-target communication though a standard RS-232 serial link. The Custom Target Board Interface kit is $30,000; this includes the first year's maintenance and customer support. SVT

***Irvine Compiler Corp., 34 Executive Park, Suite 270, Irvine, CA 92714; (714) 250-1366; fax -0676.*** **CIRCLE 807**

## DATABASE DESIGN PROGRAM UPGRADED

Version 2.0 of ModemBase Pro, a database design and display program, has been enhanced to work with both computer bulletin board systems (BBS) and as a standalone online software product. With ModemBase Pro, a user can configure most PCs to answer modem calls and log the caller directly into the database or menu of available databases. Version 2.0 remains compatible with most BBS software. The update supports the remote imaging protocol (RIP) graphical interface. ModemBase Pro 2.0 lists for $249. SVT

***Integrated Solutions, 2995 Van Buren Blvd., A-13-189, Riverside, CA 92503; (800) 633-6636; (909) 780-8860; fax -9570; BBS -5672.*** **CIRCLE 808**

D68 Series

ELECTRONIC FILTER MODULES
DIP Fixed Frequency
Up to 16 Bit Resolution

- Anti-Alias
- Noise Elimination
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- Compact size reduces board space requirements.
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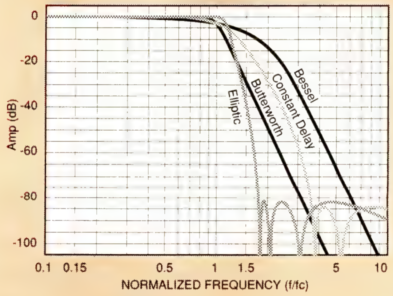
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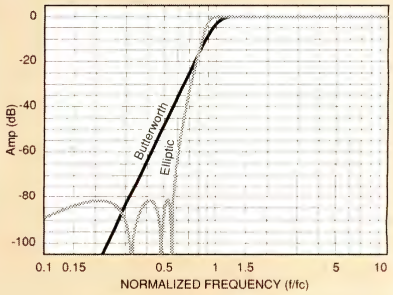
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# IBM'S EDA TECHNOLOGY IS NOW OFFERED IN SPECIALIZED PACKAGES

IBM's internal EDA tools are now available to all engineers in a series of software workbenches. The workbenches are a composition of EDA modules that solve a specific electronic-design problem. These packages provide support for major development tasks such as front-end IC design, test, physical design, and others. IBM Technology Products is offering the workbench products through the company's Altium subsidiary.

The first product, called LogicBench, is a comprehensive tool suite for VHDL-based development of complex systems and ASICs. LogicBench includes VHDL design entry, analysis, simulation, debug, and synthesis. The logic-synthesis tool, called BooleDozer, accepts both VHDL and EDIF inputs. It can optimize or synthesize at any level of a design hierarchy. In addition, it includes a set of generalized and customizable transforms that let users retarget designs across multiple installations, methodologies, design forms, and technologies.

Also available is ProFrame, an EDA framework based on the CAD Framework Initiative 1.0 standard. It also supports the MIT X-Windows standard, OSF/Motif graphical user interface, and TCP/IP and Posix to ease integration of multivendor tools and design environments. ProFrame has utility software and programming interfaces for building a common, extendible workbench that integrates diverse tools, data, and computing platforms. Its architecture separates user-oriented features from underlying application-oriented capabilities, allowing engineers to work through a consistent interface.

LogicBench will ship by the end of the year. A typical configuration goes for $127,000. ProFrame will be available in the third quarter, and costs $5500. Both products run on Unix workstations. Additional workbenches are scheduled for release over the next year.

***Altium, an IBM Co.,*** *1935 N. Buena Vista St., Burbank, CA 91504; (818) 841-9470.* **CIRCLE 809**

■ *LISA MALINIAK*

# TUNE THE PERFORMANCE OF LARGE IC DESIGNS

The Performance Engineering Toolkit (PET) from Silvar-Lisco works with the company's physical IC-design tools to ensure that large chips perform as specified. Silvar-Lisco's tools help place-and-route million-gate gate arrays and structured-custom designs. PET, which is sold as an option to this place-and-route software, helps build submicron designs that are optimized for speed, die size, and timing constraints. The toolkit consists of software that provides 100% timing coverage for all nets, built-in analog delay simulation that's accurate to Spice levels, and built-in voltage-drop analysis for supply lines. PET's automatic clock-tree synthesis minimizes skew. In addition, users enjoy a tightly-integrated synthesis-to-layout timing loop that was jointly developed with Synopsys, and also have full read and write access to the layout database. The Performance Engineering Toolkit is available now for $20,000. LM

***Silvar-Lisco, 703 E. Evelyn Ave., Sunnyvale, CA 94086; (408) 991-6000.*** **CIRCLE 810**

# TIMING ANALYZER AIDS HIGH-LEVEL DESIGN

Synopsys now offers the timing analyzer that's embedded in its synthesis environment as a standalone product called DesignTime. DesignTime is a fast, accurate static-timing analyzer that operates within its native design environment, which increases productivity and provides the necessary timing correlation. In other words, users don't have to leave their high-level design environment to perform standalone timing analysis. DesignTime uses the same graphical user interface, scripting language, and schematics as the company's high-level design tools. It links to third-party tools through a Standard Delay Format interface. A wide variety of interfaces allow it to read in and time designs and parts of designs that were not synthesized. DesignTime includes support for point-to-point timing and support for a broad range of design styles such as multiclock, multifrequency, and multiphase designs, as well as designs with both registers and latches. The tool also includes false-path management capabilities. DesignTime runs on Unix workstations, and is shipping now for $20,000. LM

***Synopsys Inc., 700 E. Middlefield Rd., Mountain View, CA 94043-4033; (415) 962-5000.*** **CIRCLE 811**

# VERILOG SIMULATION TOOLS RUN ON A PC

The VeriWell/386 Verilog-HDL simulator from Wellspring Solutions runs on 80386-, 80486-, and Pentium-based PCs under MS-DOS. VeriWell/386 is a true clone of Cadence's Unix-based Verilog-XL simulator. In fact, models were tested on both simulators to ensure compatibility. Similar user interfaces ease the transition between the two products. The 32-bit VeriWell/386 simulator supports command, input, log, and key files. In addition, it features synthesis-syntax checking, first-pass syntax and semantic error reporting, and encrypted-file support. Also, WellspringWaves is a waveform viewer that operates in the Windows-3.1 environment. It helps users debug and verify simulation results, and has an interface like that of Cadence's wave viewer. WellspringWaves supports scroll, zoom, radix change, dynamic grouping, and full control of colors and fonts. VeriWell/386 and WellspringWaves are shipping now for $995 and $449, respectively. The company also offers a 16-bit Verilog simulator for $495. LM

***Wellspring Solutions Inc., P.O. Box 150, Sutton, MA 01590; (508) 865-7271.*** **CIRCLE 812**

# FRAMEWORK TOOLKITS LET USERS BUILD CUSTOM DESIGN ENVIRONMENTS

A pair of framework toolkits from Viewlogic called ViewEDA and ViewCore let internal CAD integrators and EDA software vendors create their own custom design environments. Both toolkits use all or part of Viewlogic's OpenFrame framework technology as the underlying structure on which to build a cohesive design environment. OpenFrame supports the CFI 1.0 integration standards.

ViewEDA delivers standard integration capability that meshes third-party and in-house tools more tightly than what can be done with a net-list translation or EDIF transfer. It's comprised of a graphical cockpit, CFI-based extension language, intertool communication, and a facility to access net-list data within the database. Integrators can encapsulate tools, and can customize menus, key bindings, and dialog boxes.

ViewCore is an advanced integration package that extends the framework capabilities beyond those offered by ViewEDA. In addition to all of the ViewEDA features, ViewCore also supplies design navigation and cross-probing capabilities, access to Viewlogic's automated data-management facilities, and the ability to read and write to both the graphics and net-list databases.

Both the ViewEDA and ViewCore software tools are available now. Pricing is set at $40,000 and $90,000, respectively. Each comes with integration training by Viewlogic consultants, and telephone and field application support.

***Viewlogic Systems Inc.,** 293 Boston Post Rd. West, Marlboro, MA 01752-4615; (508) 480-0881.* **CIRCLE 813**

■ *LISA MALINIAK*

# ABEL UPGRADE ADDS VHDL DESIGN ENTRY

The latest version of the ABEL behavioral-entry design tool for programmable logic has added VHDL support. In addition, ABEL-5 has device fitters for Altera Classic, MAX 5000, and MAX 7000 families; AMD Mach 435 devices; and QuickLogic's pASIC. The VHDL-entry option, called VHDL-Direct, lets users work at a higher level of abstraction within the familiar Abel environment. VHDL-Direct supports the full spectrum of the language, including structural, RTL, and behavioral constructs. ABEL-5 can create larger, more complex designs than could previous ABEL versions thanks to increased speed, more efficient use of computer resources, and a higher level of design specificity. ABEL-5 runs on PCs. It's shipping now for $2995. LM

***Data I/O Corp., 10525 Willows Rd. N.E., P.O. Box 97046, Redmond, WA 98073-9746; (800) 332-8246 or (206) 881-6444.*** **CIRCLE 816**

# PLACE-AND-ROUTE TOOLS TARGET HIGH-END ICS

A suite of place-and-route and design-verification tools from Gambit Automated Design target complex gate arrays, standard cells, and full-custom ICs. The software can handle over a million nets and over four layers of interconnect. Gambit's tools include timing-driven layout, clock-tree synthesis, and special features for ECL technology. Parallel-processing support lets a place-and-route job automatically be distributed among several network resources. The software runs on most Unix workstations. Gambit's verification and gate-array layout tools will ship in the third quarter, and the standard-cell layout tools will be available by the end of the year. Also planned are floorplanning tools, which will team with the standard-cell software for full-custom design capability. Call the company for pricing and additional information. LM

***Gambit Automated Design Inc., 1245 S. Winchester Blvd., Suite 220, San Jose, CA 95128; (408) 345-3555.*** **CIRCLE 814**

# ON-LINE SERVICE GIVES COMPONENT INFORMATION

EnGenius is an on-line engineering-information service that offers text and graphics describing technical data for thousands of semiconductor and electronic components. The service also has ASIC specifications, symbols, models, and other CAE-usable information. It will be electronically updated daily by manufacturers to maintain currency. Engineers can do searches by part number, function, and parametrics. Then, they can print information and download CAE-usable data. Future capabilities include video, audio, electronic mail, individual and group annotations, and change notifications. EnGenius Release 1.0 is available on Unix workstations. Future releases will also support personal-computer and Macintosh platforms. Current access is via modem. The average end-user price is estimated at $49 per month. LM

***Info Enterprises Inc., a Motorola Co., 3260 N. Colorado St., Chandler, AZ 85225-1123; (800) 851-7536 or (602) 545-6340.*** **CIRCLE 815**

# VERTICAL TOOLKITS OPTIMIZE MCM DESIGN

Vertically-integrated MCM toolkits from Cadence help eliminate the complexity, technology-transfer, and cost obstacles that plague mainstream users. Technology partnerships with IBM Technology Products, Kyocera, and Toshiba have allowed Cadence to create software that shortens the overall MCM design cycle—from concept through fabrication. The MCM solutions are based on Cadence's Allegro MCM Design System. Common technology specifications such as power, cost, die size, and clock rates guide users through an automatic selection of the best-suited foundry design kit. Once the choice is made, the EDA environment is automatically programmed for that selection. The vertical MCM solutions run on Unix workstations, and are available now. Prices start at $99,000. LM

***Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234.*** **CIRCLE 817**

## CHARGER-IC BOARD SIMPLIFIES INTEGRATION

Easier, less-costly prototyping of battery-charging systems is now possible with the ECS-Heartprint circuit board. The Heartprint board integrates the Enstore ECS-II battery-charging IC *(Electronic Design, June 10, p. 120)* as well as most of the external components necessary to build a finished product. These include a voltage regulator, resistor network, filter capacitor, and a 100-mA driving transistor for the external power transistor. The board's small size (51 by 18 by 5 mm) also makes it useful for space-limited applications including cellular phones, notebook computers, personal digital assistants, and other portable equipment in commercial and consumer areas. Chargers built with the board can be configured to work with lead-acid, nickel metal hydride, and nickel cadmium batteries. Other options let users quickly select the number of cells, rate of maximum charging current, and charge-maintenance techniques. Pricing is as low as $16 in large quantities. Call for delivery information. DM

***EnChip Inc., 434 Ridgedale Ave., Suite 11-327, East Hanover, NJ 07936; Jerry Eisenband, (201) 328-2049.*** **CIRCLE 818**

## DENSE DC-DC SUPPLIES MEET QUASI-MIL NEEDS

Single- and triple-output dc-dc converters with power density of 58 W/in.$^3$ are available in a quasi-MIL version, with a fully qualified MIL version to come. The HDM Series supplies' single-output versions offer 5 V at 40 A, 12 V at 20 A, 15 V at 16 A, 24 V at 10 A, or 28 V at 9 A. Triple-output models supply 5 and ±12 V dc or 5 and ±15 V dc. Nominal dc-input voltages are 28, 48, or 300 V. Maximum outputs are 250 W for single outputs and 185 W for the three-output types. Call for pricing. DM

***Rantec Microwave & Electronics Inc., 24003 Ventura Blvd., Calabasas, CA 91302; (818) 591-8189.*** **CIRCLE 820**

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## IGNITION PREDRIVER CLOSELY CONTROLS SPARK

Driving of external power transistors, including IGBTs in an automotive-ignition control module, is accomplished by the 67F6612 ignition-predriver IC. Precision dwell and current-limit thresholds provide accurate spark control for a broad range of engine applications. A single logic-level input for each channel controls the IC's functions. A four-channel version comes in 20-pin SO and VSOP packages, while three- and two-channel types come in 16- and 14-pin packages, respectively. In large OEM lots, pricing is under $3. Call for delivery information. DM

***Silicon Systems, 14351 Myford Rd., Tustin, CA 92680; (800) 624-8999, ext. 151.*** **CIRCLE 821**

## AXIAL-LEAD SUPPRESSORS QUASH VOLTAGE SPIKES

Protection of semiconductors and other voltage-sensitive devices from transients is provided by a line of axial-lead transient-voltage-suppressor diodes. The devices are specially designed for through-hole applications and are easily handled by automatic assembly equipment. They're characterized by fast response times of $1\times10^{-12}$ s, resulting in the lowest possible clamping voltage. Three series are available: the SA Series (rated at 500 W), the P6KE Series (600 W), and the 1.5KE Series (1500 W). Pricing is as low as $0.26 for lots of 10,000. Delivery of small lots is from stock. DM

***Semtech Corp., 652 Mitchell Rd., Newbury Park, CA 91320; Mamoon Rashid, (805) 498-2111.*** **CIRCLE 822**

## 3-BY-3-IN CONVERTER PROVIDES UP TO 60 W

Fifty to 60 W of output power is delivered by the TT Series of 3-by-3-in. dc-dc converters. The six 24- and 48-V models offer a power density of nearly 10 W/in.$^3$. There are two 2:1 input ranges to choose from: 18 to 36 V or 36 to 72 V, each with the option of 5 V at 10 A, 12 V at 5 A, or 15 V at 4 A. Other key features include efficiencies to 83%, input-to-output isolation of 1544 V dc for 48-V models and 700 V dc for 24-V models, a logic on-off pin to conserve power, and continuous short-circuit protection. Samples are available from stock with OEM quantities being delivered in from four to six weeks. Pricing is $60 in large lots. DM

***Calex Mfg. Co. Inc., 2401 Stanwell Dr., Concord, CA 94520-4841; Stu Williams, (510) 687-4411.*** **CIRCLE 823**

## 1200-W MODULAR SUPPLY HAS FULL FEATURE SET

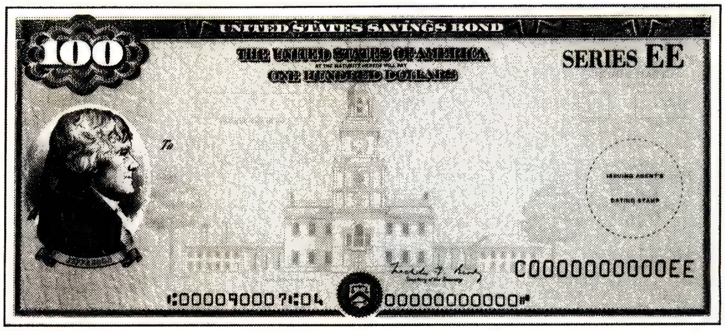
A fully modular architecture that permits quick configuration to specific user requirements is just one feature of the Unimod HPB Series of switching power systems. The series, which has six module slots and 25 available output modules with outputs from 80 to 1200 W, incorporates such features as power-factor correction to 0.98, input autoranging for worldwide operation, a VDE Level B input-EMI filter, and a battery-backup module. A full set of protection features is also included, as is optional current sharing. Unit prices start at $1405 with OEM pricing at $1037. Samples are available in two weeks with production deliveries in four to eight weeks. DM

***Unipower Corp., 2981 Gateway Dr., Pompano Beach, FL 33069; Warren Peters, (305) 974-2442.*** **CIRCLE 824**

## 3-PHASE IGBT MODULE DRIVES INVERTERS

A 600-V, 100-A, three-phase IGBT module is available for driving brushless motors, inverters, and power supplies. The EFMT-M338 module is also offered in a 1200-V model and in several circuit configurations for low- and high-side choppers in conjunction with reluctance drives. Sense custom models are also available with built-in snubbers and gate drivers in the same package. Power-MOSFET output devices can also be used in place of the IGBTs. Call for pricing. DM

***Gentron Corp., 7345 E. Acoma, Suite 101, Scottsdale, AZ 85260; (602) 443-1288.*** **CIRCLE 825**



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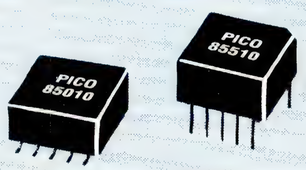

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# PCMCIA-CREDIT-CARD-SIZED PC PACKS A FULL 386-PROCESSOR SYSTEM

Taking aim at consumer equipment and portable computers, designers at Seiko Epson and S-MOS Systems have created a full 386-based PC in the space occupied by a PCMCIA memory card (about the size of a credit card). The CARDIO computer module—the SCE86325—includes the CPU (80386SL), I/O controls (82360SL), disk controller, graphics control, keyboard interface controller, BIOS, memory, and many other features.

The small format of the card permits the computer to readily be embedded in a wide variety of systems. These include point-of-sale terminals, factory automation hardware, hand-held terminals, instrumentation, VCRs, facsimile machines, and even smart vending machines.

The card measures 85.4-by-54-by-5.5-mm and its computer inside is fully IBM PC-AT compatible, able to operate at clock speeds of 16 or 20 MHz. A special 236-pin connector interface on the long edge of the card provides access to all the functions on the CARDIO, including the ISA and I/O ports. In contrast, PCMCIA cards have the connector on the short end and typically only use a 68-pin connection. Additional versions of the card that employ 8086 and 80486 CPUs are also in development.

Versions of the CARDIO will be available with 1, 2, or 4 Mbytes of RAM, and 128 or 256 kbytes of ROM (for BIOS storage). The VGA output port can drive either an analog RGB monitor or monochrome super-twist mnematic or color TFT LCD displays. The card can run from either a 3.3-V +/-0.3-V or a 5-V +/-5% power supply, and the BIOS includes VGA as well as power-management support.

Depending on configuration and clock speed, prices for the CARDIO start at less the $400 apiece in lots of 1000. Evaluation kits that include some peripherals (hard-disk and floppy disk drives, LCD panel, etc.) and other functions have single-unit prices ranging from $900 to $2300, depending on peripherals.

*S-MOS Systems, 2460 N. First St., San Jose, CA 95131-1002; (408) 922-0200.* **CIRCLE 826**

■ *DAVE BURSKY*

# VME CPU BOARD HOLDS FIVE DSP CHIPS

The AP655 high-performance signal-processing board is built with five TI 40-MHz TMS320C31 DSP chips. The 6U VME board delivers 200 MFLOPS of performance for applications that require high-performance pipeline or multi-channel processing with wide-band I/O. The efficient address-pipelined memory architecture effectively hides the global memory wait states from the application process. The advanced global memory also minimizes access conflicts and collisions in a multiprocessor environment. To maximize I/O performance, the five TI DSP engines are arranged in a master-slave configuration with all processors acting as computational peers. The master processor controls most of the I/O functionality, including an 80-Mbyte/s bidirectional FIFO port that connects to external devices. For OEM applications, the AP655 can be customized using daughtercards. With 16 Mbytes of memory, the board is priced at $13,200. Large quantity discounts are available. RN

***Analogic Corp., 8 Centennial Dr., Peabody, MA 01960; (508) 977-3000.*** **CIRCLE 827**

**Correction**

In our Aug. 19 issue (p. 122), the phone number listed for the IMAXX boards from Precision Digital Images Corp. (Redmond, Wash.), which are capable of capturing images up to 2K by 2K by 8 bits, should have been 206-882-0218.

## IC DATABOOK

A comprehensive, long-form databook from Harris Semiconductor, Melbourne, Fla., describes hundreds of linear and telecommunications-specific standard ICs. The databook, "Linear & Telecom ICs for Analog Signal Processing Applications 1993-94," includes extensive application information, including sections on operational amplifiers; comparators; sample and hold amplifiers; transistor and diode arrays; special analog circuits; and telecommunications ICs, such as subscriber line interface circuits and crosspoint switches. Additional sections include SPICE model listings, abstracts for long-form application notes, quality and reliability data, and packaging and ordering information. Designers can obtain the databook by called by calling 1-800-HARRIS, ext. 7115.

**CIRCLE 899**

## CATALOG DETAILS SENSORS

Optek Technology's 800-page catalog describes infrared sensors, magnetic sensors, fiber-optic sensors, and the Hi-Rel series. The catalog also has new application bulletings, data sheets, and a product-selection guide. Contack Optek (214) 323-2200. SVT **CIRCLE 900**

## UNINTERRUPTIBLE SYSTEMS

A highly informative brochure on interruptible ac-dc power systems from Transistor Devices Inc., Randolph, N.J., serves design engineers as a complete reference on the subject. One of the main areas of focus is fault-tolerant, zero-down-time systems incorporating N+1 and 2N redundancy architectures, power-factor correction, and built-in test.

Other sections cover uninterruptible-system design, alternate design configurations, and protective features and fault alarms. Extensive coverage is also given to battery characteristics for both lead-acid and nickel cadmium types. There are many illustrations included to show technical characteristics. CM

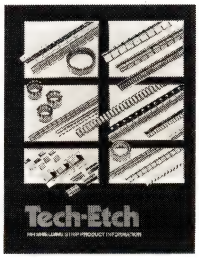
**CIRCLE 901**

## LINEAR & TELECOM IC DATABOOK

A long-form databook from Harris Semiconductor, Melbourne, Fla., describes hundreds of linear and telecommunications-specific standard ICs. The free databook, Linear & Telecom ICs for Analog Signal Processing Applications, which includes extensive application information, contains sections on operational amplifiers, comparators, sample and hold amplifiers, differential amplifiers, transistor and diode arrays, special analog circuits, and telecommunications ICs.

Additional sections include SPICE model listings, abstracts for long-form application notes, quality and reliability data, and packaging and ordering information. Call 1-800-4-HARRIS, ext. 7115. CM **CIRCLE 902**

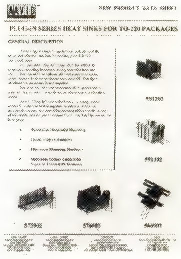
## EMI/RFI SHIELDING COMES IN WIDE VARIETY



Beryllium copper EMI/RFI-shielding products are the subject of a 20-page catalog from Tech-Etch Inc., Plymouth, Mass. The free catalog contains general information on a wide variety of shielding strips, including soft fingers, no-snag fingers, omni contacts, panel gaskets, reverse-bend and twisted contacts, and many more.

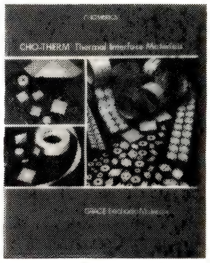
Specifications given include full-size technical drawings, compression values, special finishes, standard and custom options, as well as ordering information. DM **CIRCLE 903**

## TO-220 HEAT SINKS ARE BULLETIN'S SUBJECT



Heat sinks for cooling TO-220 semiconductor packages are the subject of a four-page product bulletin from Aavid Engineering Inc., Laconia, N.H. The heat sinks feature a labor-saving design that enables TO-220s to be plugged in quickly, eliminating time-consuming fastening with nuts and bolts. The sinks' fins form spring-action clips that hold the package securely, providing a tight fit for maximum surface contact and superior thermal performance. DM **CIRCLE 904**

## THERMAL CONDUCTORS DESCRIBED IN BROCHURE

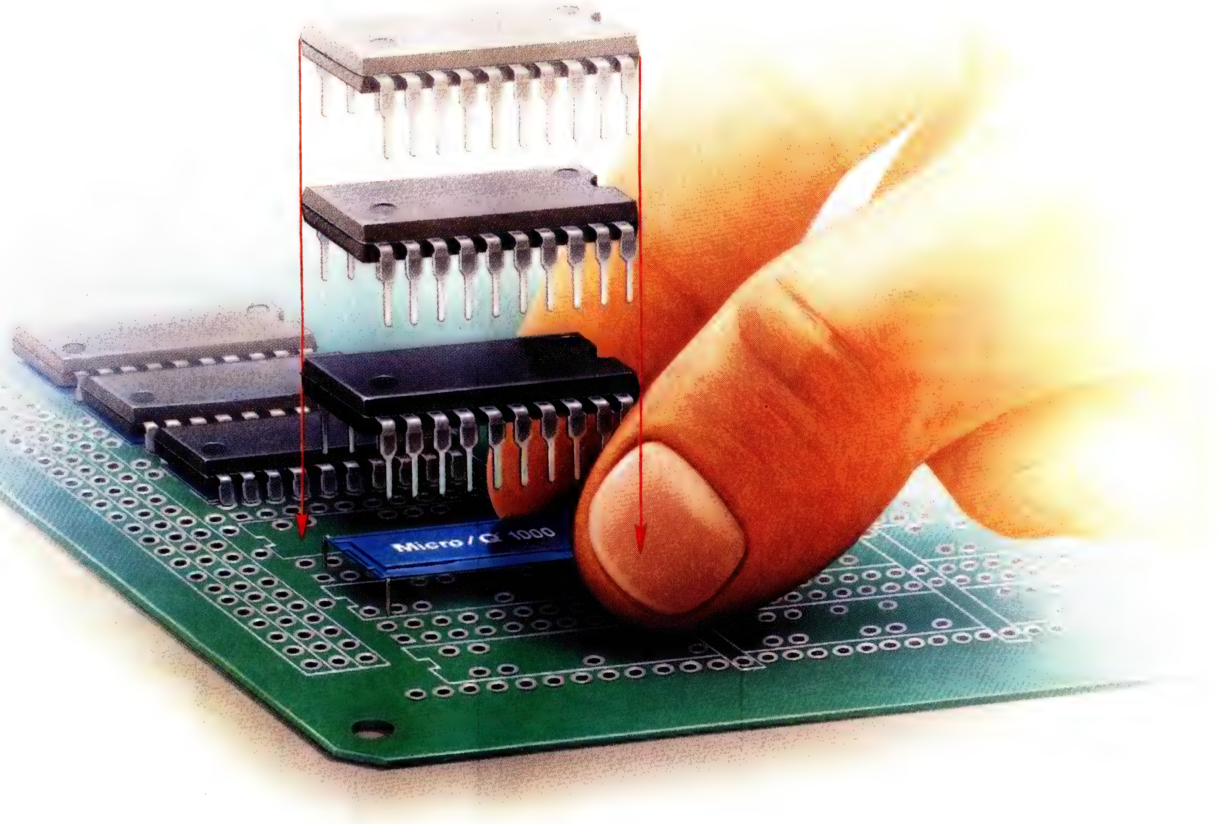


The Cho-Therm family of thermal-interface materials is described in a 20-page brochure from Chomerics Inc., Woburn, Mass. The brochure profiles thermally conductive insulators, mounting pads, adhesive tapes, conformable gap fillers, and potting compounds. It also features new products such as Thermattach double-sided adhesive tapes, Cho-Therm T500 chiller-plate insulators, and ribbed forms of Cho-Therm gap fillers. Configuration charts provide dimensions and part numbers. DM

**CIRCLE 905**

## CATALOG DESCRIBES TEST EQUIPMENT

A catalog from National Electric and Instrumentation, Elizabeth, N.J., details descriptions of electronic test equipment and service tools from many manufacturers. The catalog lists DMMs, component testers, scopes, signal generators, counters, dc power supplies, programmers, and specialty products. JN **CIRCLE 906**



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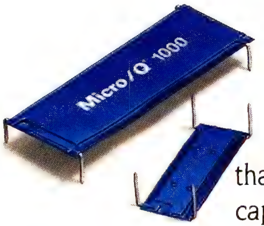

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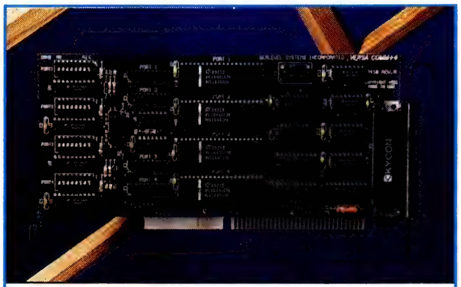

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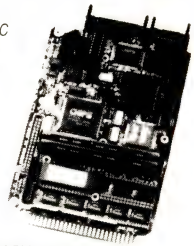

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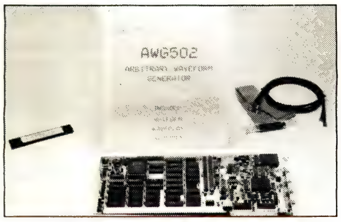

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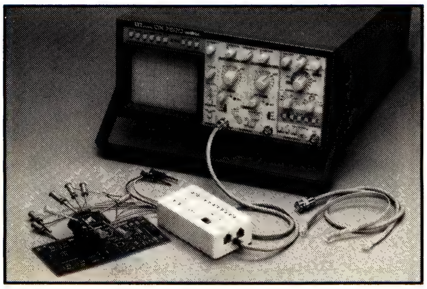

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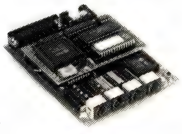

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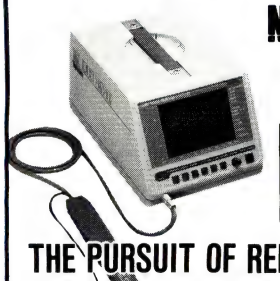

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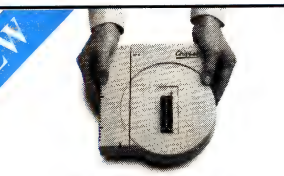

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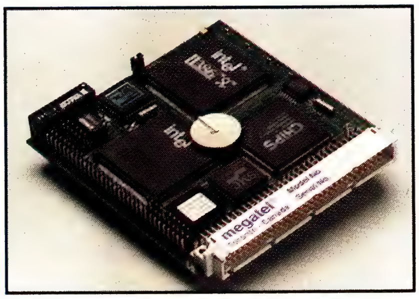

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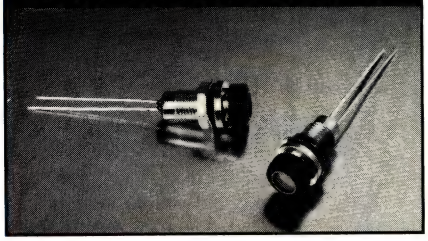

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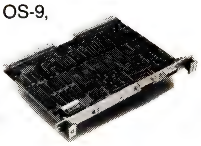

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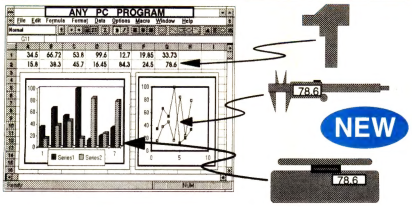

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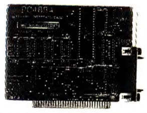

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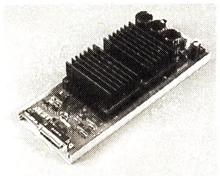

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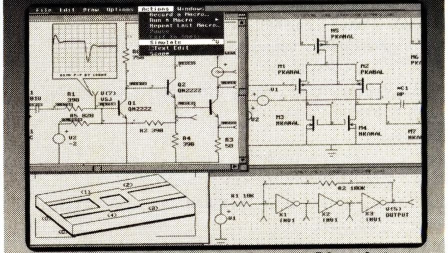

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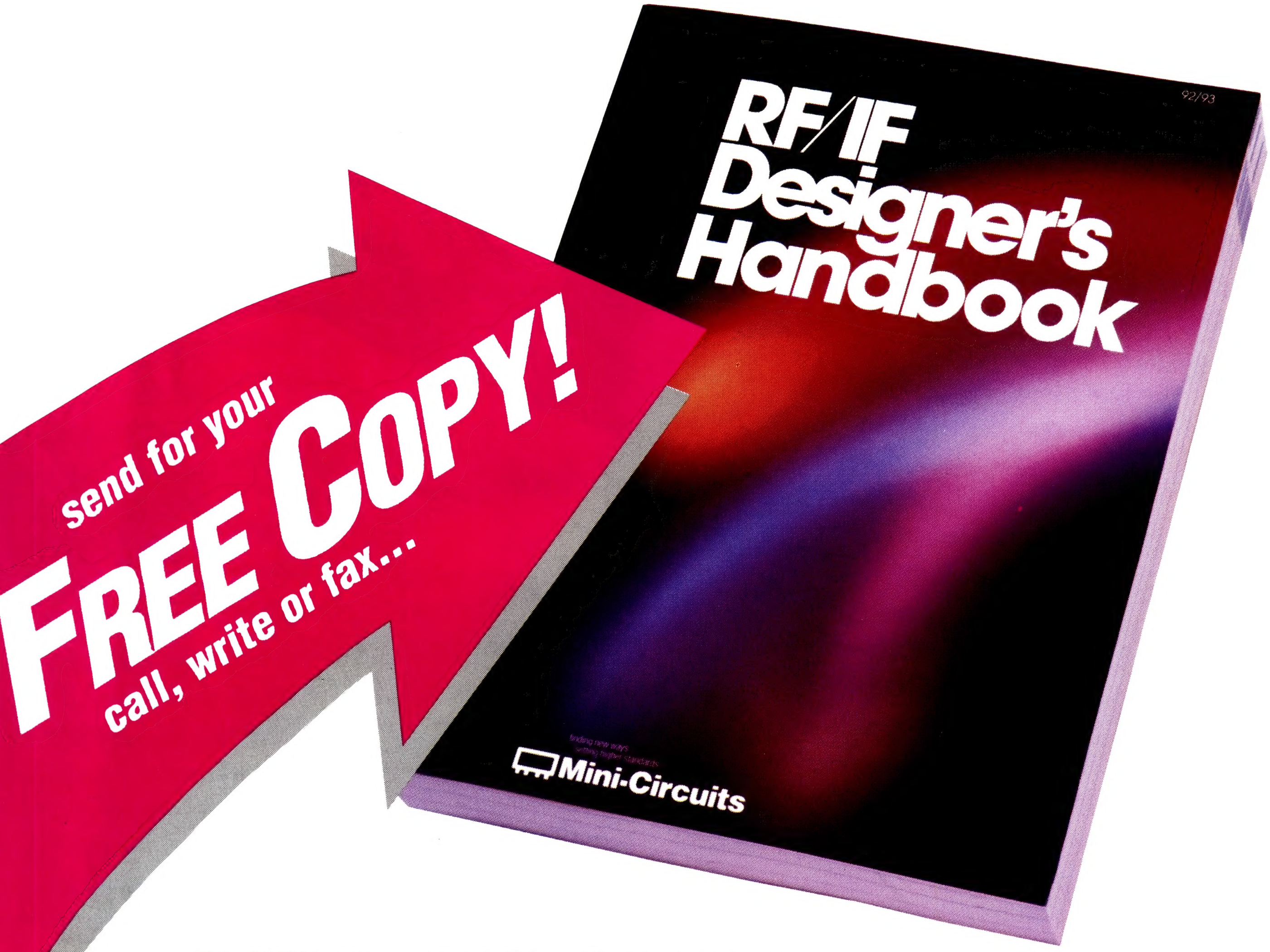
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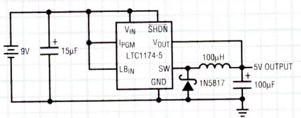

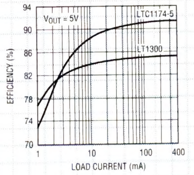

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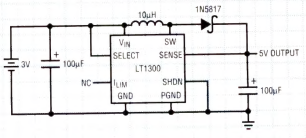

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